IG1NT052N10R (JANSG2N7697UFHC)

PD-98011C

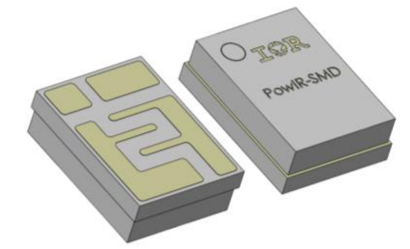
Radiation Hardened GaN transistor
Surface Mount (PowIR-SMD)
100V, 52A, N-channel, Enhancement mode

Features

- Single event effect (SEE) hardened
  up to LET (GAN)[1] = 70 MeV.cm^2/mg (Au ion)
- Ultra low $R_{DS(on)}$
- Low total gate charge
- Zero reverse recovery charge
- Hermetically sealed ceramic package
- Surface mount
- Light weight
- ESD rating: Class 1C per MIL-STD-750, Method 1020

Product Summary

- **$V_{DS\ max}$**: 100V
- **I_D**: 52A
- **$R_{DS(on)\ max}$**: 6.0mΩ
- **$Q_{G\ max}$**: 13nC
- **Size:** 7.1mm x 5.3mm
- **REF:** MIL-PRF-19500 / 794



PowIR-SMD

Potential Applications

- Isolated DC-DC converters
- Point-of-load (PoL) converters for FPGA, ASIC and DSP core rails
- Synchronous rectification
- Motor drives

Product Validation

Validated based on MIL-PRF-19500 for space applications

Description

IG1NT052N10R is part of the IR HiRel family of products. IR HiRel radiation hardened GaN transistor technology provides high performance power devices for space applications. These devices have been characterized for both Total Ionizing Dose (TID) and Single Event Effects (SEE). The combination of low $R_{DS(on)}$, low gate charge and zero reverse recovery charge reduces the power losses in switching applications such as DC-DC converters and motor control. These devices enable high-frequency operation of power management circuits resulting in high-power density and low payload mass.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IG1NT052N10R	PowIR-SMD	COTS	100 krad(Si)
IG1NT052N10G	PowIR-SMD	COTS	500 krad(Si)
JANSG2N7697UFHC	PowIR-SMD	JANS	500 krad(Si)

[1] LET Si equivalent = 86.5 MeV.cm^2/mg

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{DS}	Continuous Drain-to-Source Voltage	—	—	100	V	V_{GS} = 0V, I_D = 0A
$V_{DS, pulse}$	Pulsed Drain-to-Source Voltage [1]	—	—	120	V	V_{GS} = 0V, 1h total time
I_{D1}	Continuous Drain Current	—	—	52	A	V_{GS} = 5V, T_C = 25°C
I_{D2}	Continuous Drain Current	—	—	33	A	V_{GS} = 5V, T_C = 100°C
$I_{D, pulse}$	Pulsed Drain Current[2]	—	—	208	A	T_C = 25°C
V_{GS}	Pulsed Gate-source Voltage [1]	-6.5	—	+6.5	V	Pulsed 100h total time
P_D	Maximum Power Dissipation	—	—	30	W	T_C = 25°C
	Linear Derating Factor	—	—	0.24	W/°C	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55	—	150	°C	
	Package Mounting Surface Temperature	—	—	300	°C	for 5s
	Weight	—	—	0.23	g	

2 Recommended Operating Conditions

Table 3 Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{GS}	Gate-Source voltage (DC)	-5.0	4.8	5.1	V	
V_{GS}	Gate-Source voltage (transient)[3]	-5.5	—	5.5	V	

[1] Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.
[2] Repetitive Rating; Pulse width limited by maximum junction temperature.
[3] Pulse width < 50 ns

3 Device Characteristics

3.1 Electrical Characteristics (Pre-Irradiation)

Table 4 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$V_{DS\ max}$	Drain-to-Source Voltage, continuous	—	—	100	V	V_{GS} = 0V, I_D = 0A
$R_{DS\ (on)}$	Static Drain-to-Source On-State Resistance	—	4.0	6.0	mΩ	V_{GS} = 5V, I_D = 33A [1]
$V_{GS\ (th)}$	Gate Threshold Voltage	1.0	1.5	2.0	V	V_{DS} = V_{GS}, I_D = 8.0mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.0	—	mV/°C	
I_{DSS}	Zero Gate Voltage Drain Current	—	0.1	10	µA	V_{DS} = 100V, V_{GS} = 0V
		—	10	100		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	0.03	0.5	mA	V_{GS} = 5.0V, T_J = 25°C
			0.5	1		V_{GS} = 5.0V, T_J = 125°C
	Gate-to-Source Leakage Reverse	—	0.2	1	µA	V_{GS} = -5.0V, T_J = 25°C
			2.5	10		V_{GS} = -5.0V, T_J = 125°C
R_G	Gate Resistance	—	1.5	—	Ω	f = 1.0MHz, open drain
Q_G	Total Gate Charge	—	8.8	13	nC	I_D = 33A V_{DS} = 50V V_{GS} = 5.0V
Q_{GS}	Gate-to-Source Charge	—	3.1	—		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	1.1	—		
Q_{OSS}	Output Charge	—	44	—	nC	V_{DD} = 50V, V_{GS} = 0V
C_{iss}	Input Capacitance	—	820	—	pF	V_{GS} = 0V V_{DS} = 50V f = 1.0MHz
C_{oss}	Output Capacitance	—	510	—		
C_{rss}	Reverse Transfer Capacitance	—	7.7	—		

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

3.2 Reverse Operation - Ratings and Characteristics (Pre-Irradiation)

Table 5 Reverse Operation Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current	—	—	52	A	$T_J = 25°C$
I_{SM}	Pulsed Source Current [1]	—	—	208	A	$T_J = 25°C$
V_{SD}	Forward Voltage	—	2.1	3.9	V	$T_J = 25°C$, $I_S = 33A$, $V_{GS} = 0V$ [2]
Q_{rr}	Reverse Recovery Charge	—	0	—	nC	$T_J = 25°C$, $I_S = 33A$, $V_{DD} = 50V$ $di_S/dt = 100A/\mu s$

3.3 Thermal Characteristics

Table 6 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	1.9	4.0	°C/W
$R_{\theta J\text{-}PCB}$	Junction-to-Case-with Heat Sink	—	20	25	
$R_{\theta JA}$	Junction-to-Ambient -Devices on PCB (in free air)	—	45	70	

3.4 Radiation Characteristics

IR HiRel Radiation Hardened GaN transistors are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4.) Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

3.4.1 Electrical Characteristics - Post Total Dose Irradiation

Table 7 Electrical Characteristics @ $T_J = 25°C$, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 500 krad (Si) [5]		Unit	Test Conditions
		Min.	Max.		
$V_{DS\,max}$	Drain-to-Source Breakdown Voltage	100	—	V	$V_{GS} = 0V$, $I_D = 0A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0	V	$V_{DS} = V_{GS}$, $I_D = 8.0mA$
I_{GSS}	Gate-to-Source Leakage Forward	—	0.5	mA	$V_{GS} = 5V$
	Gate-to-Source Leakage Reverse	—	1.0	µA	$V_{GS} = -5V$
I_{DSS}	Zero Gate Voltage Drain Current	—	10	µA	$V_{DS} = 100V$, $V_{GS} = 0V$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (Package PowIR-SMD) [2]	—	6.0	mΩ	$V_{GS} = 5V$, $I_D = 33A$
V_{SD}	Source-Drain Forward Voltage	—	3.9	V	$V_{GS} = 0V$, $I_S = 33A$

[1] Repetitive Rating; Pulse width limited by maximum junction temperature
[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
[3] Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 5V$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.
[4] Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 80V$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.
[5] Part numbers IG1NT052N10R (100 krad(Si)) and IG1NT052N10G (JANSG2N7697UFHC) 500 krad(Si)

3.4.2 Single Event Effects – Safe Operating Area

IR HiRel radiation hardened GaN transistors have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Figure 1 and Table 8.

Table 8 Typical Single Event Effects Safe Operating Area

Ion	LET (GaN)[1] (MeV.cm^2/mg)	Energy (GaN) (MeV)	Range (GaN) (µm)	V_{DS} (V)	
				V_{GS} = 0V	V_{GS} = -5V
Au	70 ± 5%	1713 ± 5%	48 ± 5%	100	100

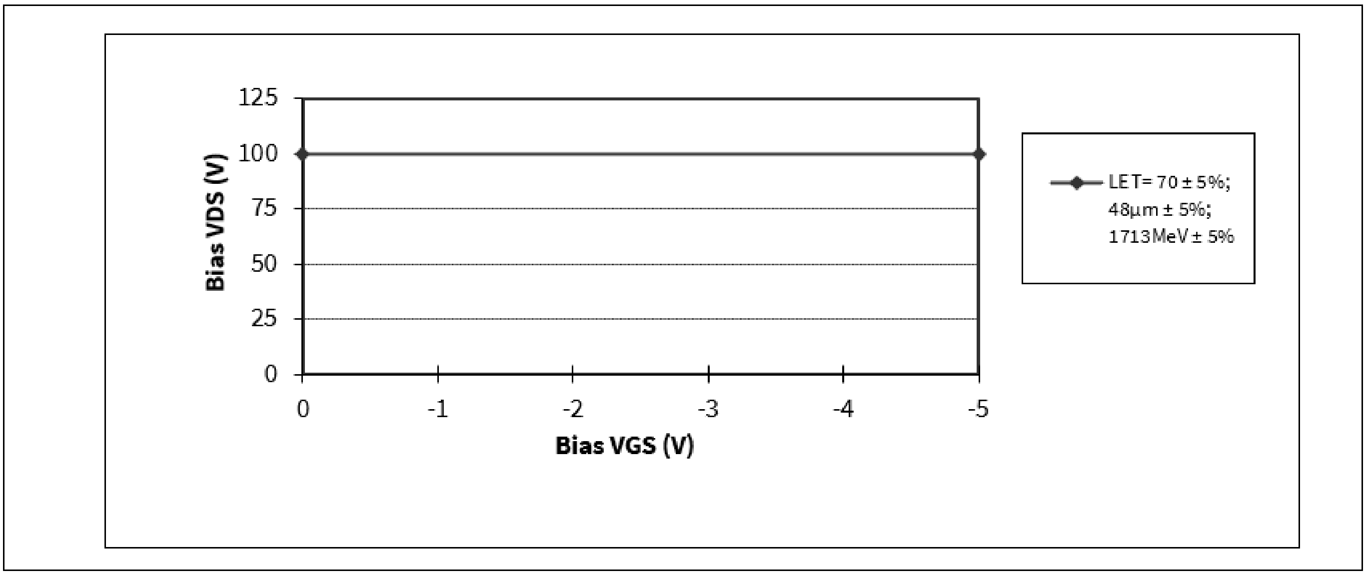


Figure 1 Typical Single Event Effect, Safe Operating Area

[1] LET Si equivalent = 86.5 MeV.cm^2/mg

4 Electrical Characteristics Curves (Pre-irradiation)

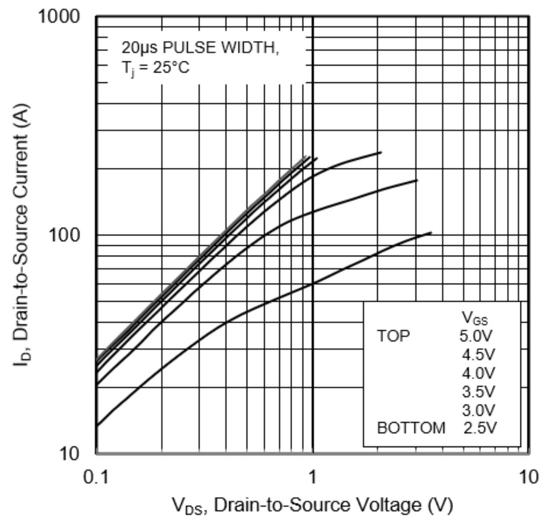


Figure 2 Typical Output Characteristics

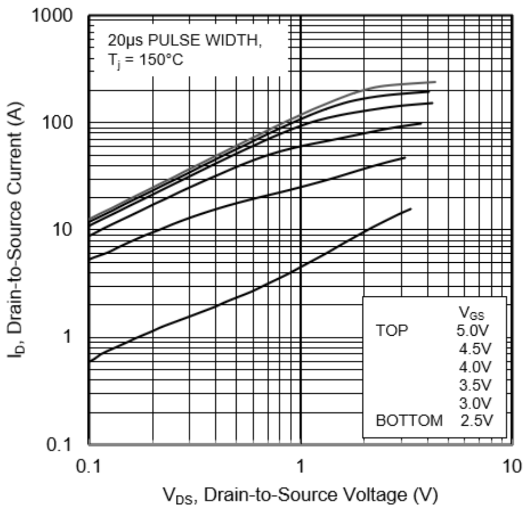


Figure 3 Typical Output Characteristics

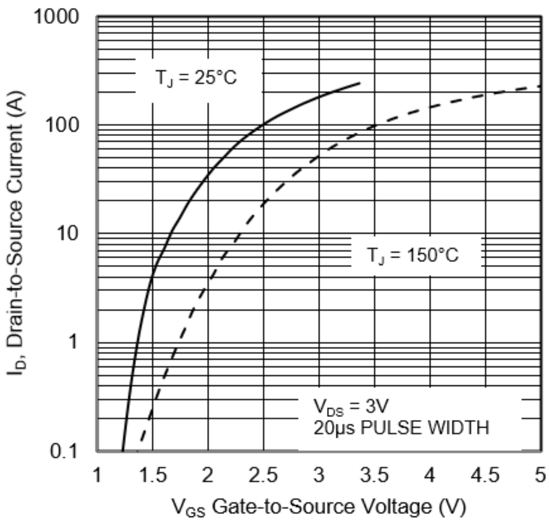


Figure 4 Typical Transfer Characteristics

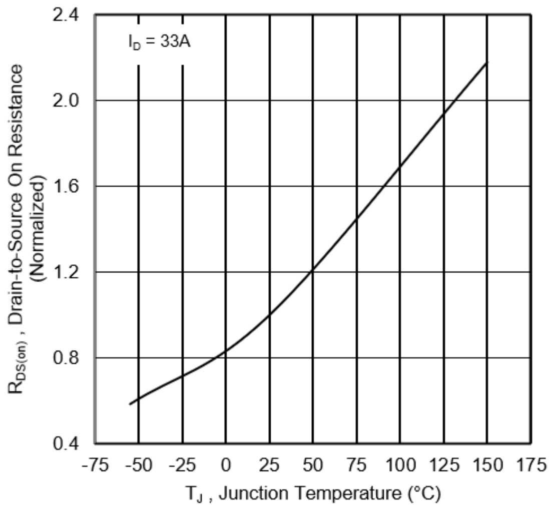


Figure 5 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

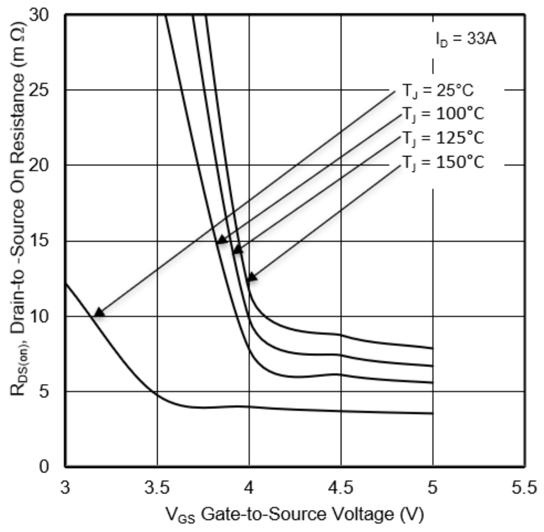


Figure 6 **Typical On-Resistance Vs. Gate Voltage**

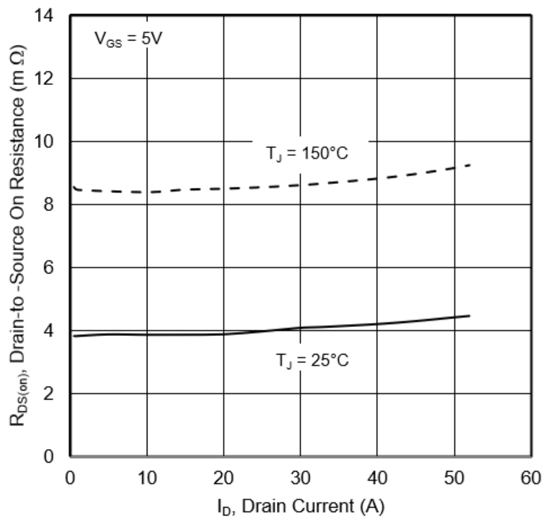


Figure 7 **Typical On-Resistance Vs. Drain Current**

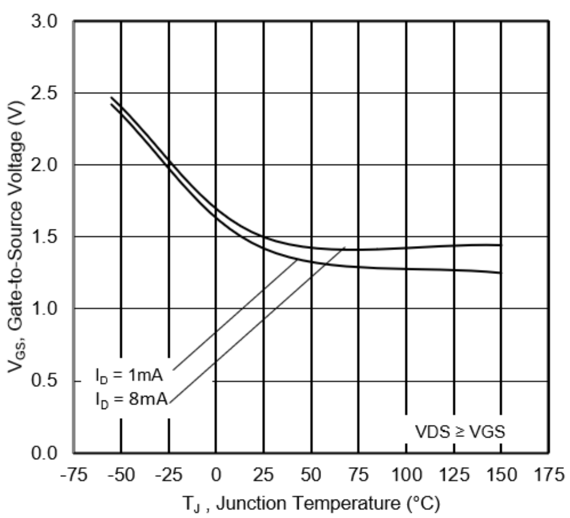


Figure 8 **Typical Threshold Voltage Vs. Temperature**

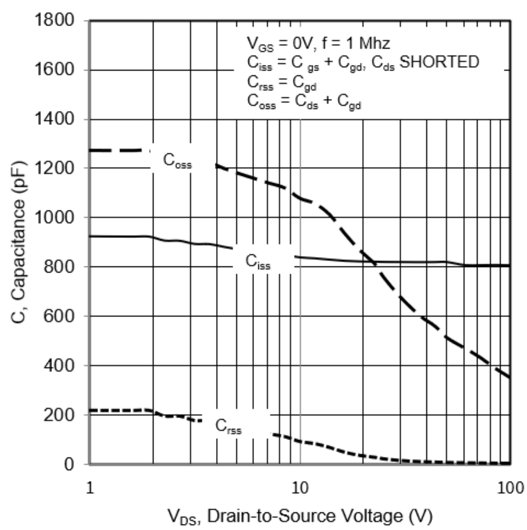


Figure 9 **Typical Capacitance Vs. Drain-to-Source Voltage**

Electrical Characteristics Curves (Pre-irradiation)

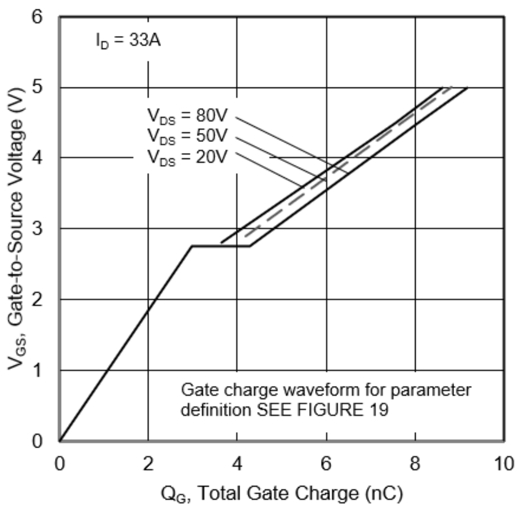


Figure 10 **Typical Gate Charge Vs. Gate-to-Source Voltage**

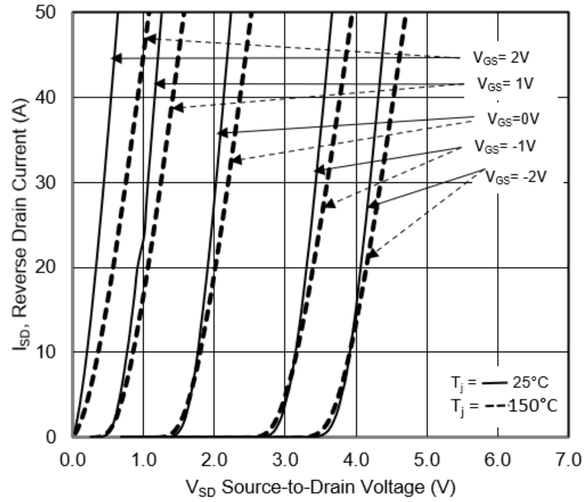


Figure 11 **Typical Source-Drain Current Vs. Source-Drain Voltage (reverse output characteristics)**

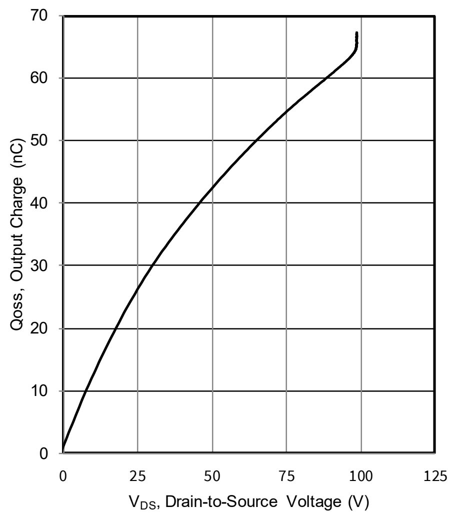


Figure 12 **Typical Output Charge**

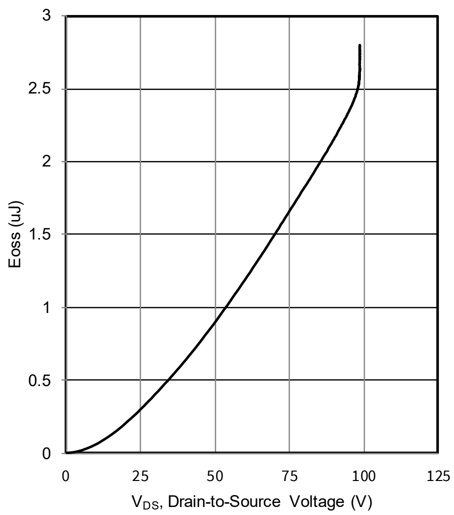


Figure 13 **Typical Output Energy**

Electrical Characteristics Curves (Pre-irradiation)

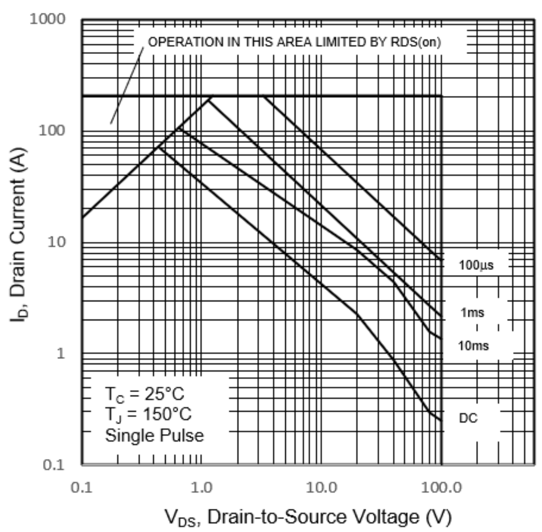


Figure 14 Maximum Safe Operating Area

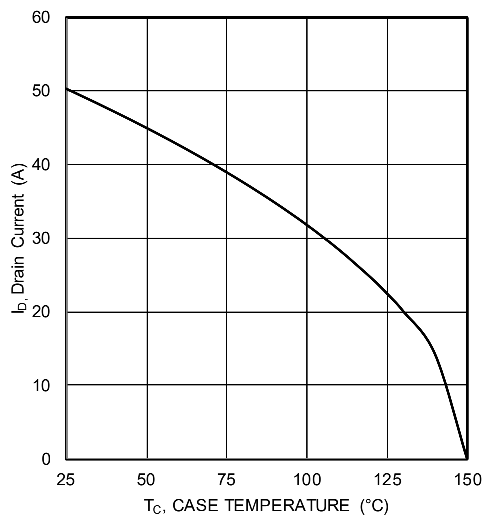


Figure 15 Maximum Drain Current Vs. Case Temperature

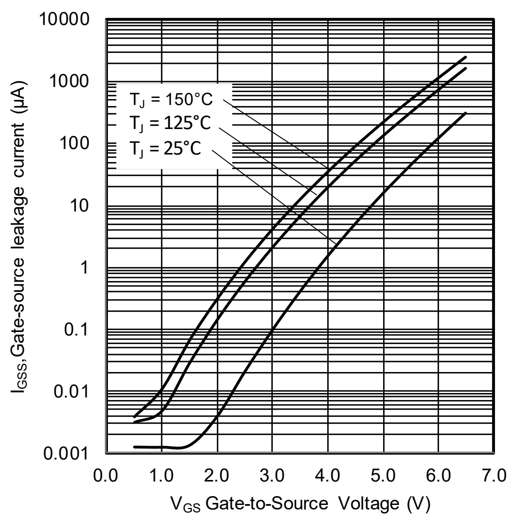


Figure 16 Typical Gate-Source Leakage Current Vs. Gate-Source Voltage (Positive voltage)

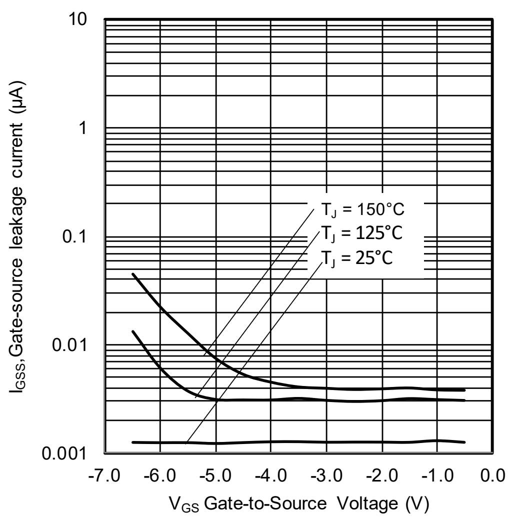


Figure 17 Typical Gate-Source Leakage Current Vs. Gate-Source Voltage (Negative Voltage)

Electrical Characteristics Curves (Pre-irradiation)

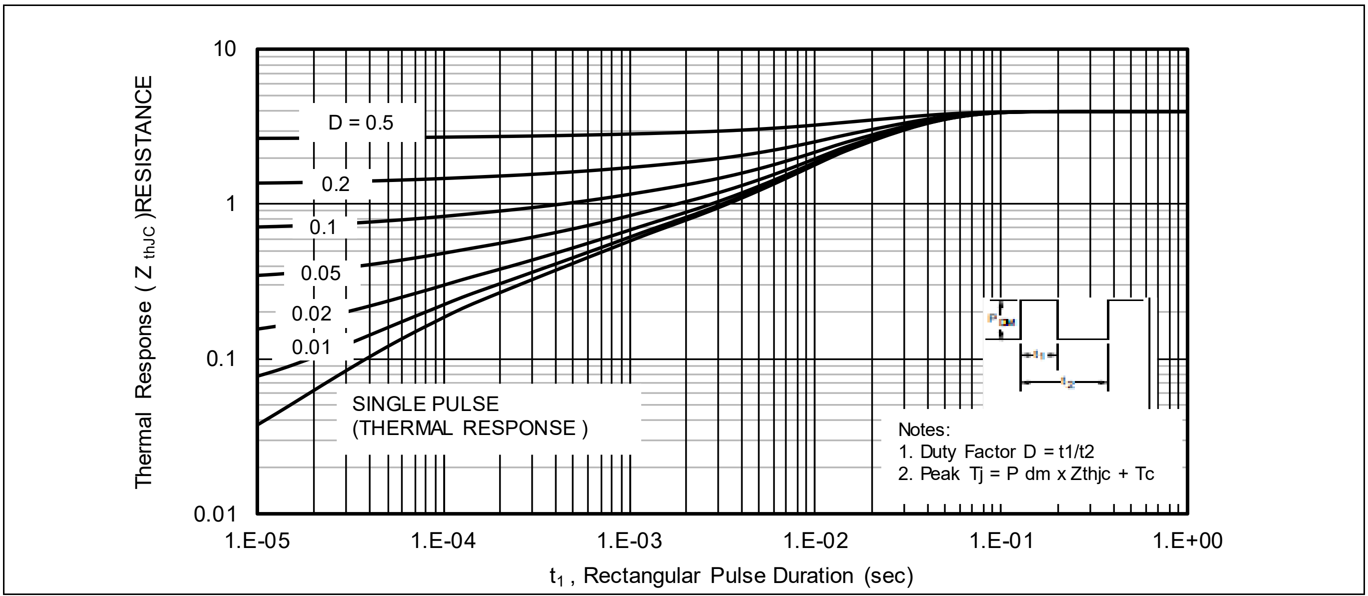


Figure 18 Maximum Effective Transient Thermal Impedance, Junction-to-Case

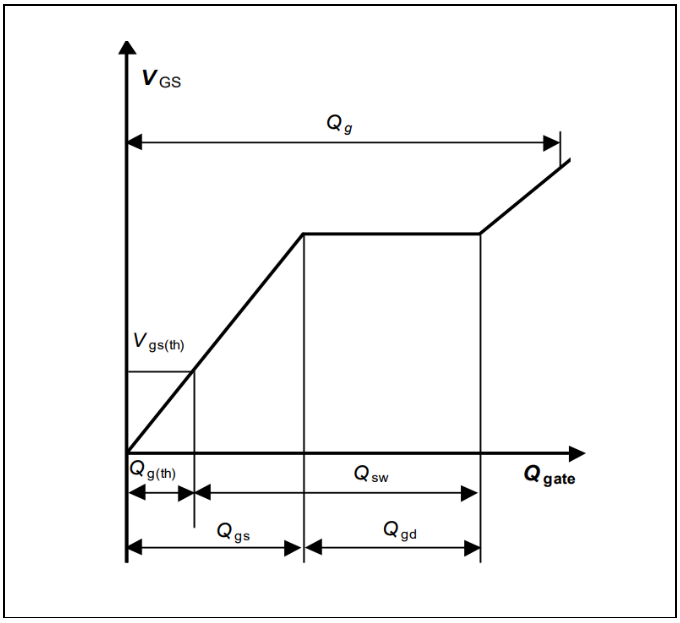
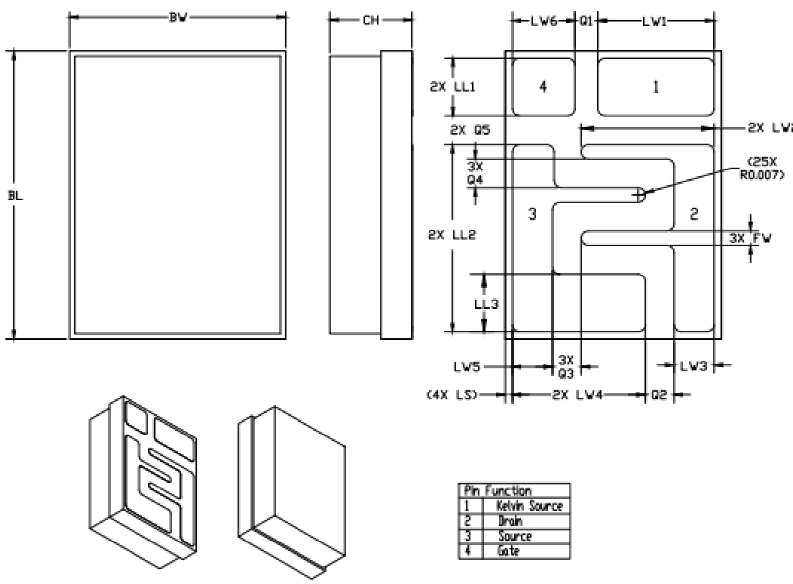


Figure 19 Gate Charge Waveform

5 Package Outline

Note: For the most updated package outline, please see the website: PowIR-SMD

REV.	DESCRIPTION	ECN	DATE
C	CHANGE PER ECN	Z8F80855955	10-14-25



Pin	Function
1	Kelvin Source
2	Drain
3	Source
4	Gate

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M.
2. CONTROLLING DIMENSION: INCHES
3. LEAD PLATING IS GOLD. STANDARD FINAL LEAD FINISH IS SOLDER ALLOY 63Sn/37Pb. DIMENSIONS APPLY BEFORE SOLDER FINISH.

DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
BL	.275	.280	.285	6.99	7.11	7.24
BW	.205	.210	.215	5.21	5.33	5.46
CH			.100			2.54
LL1	.051	.056	.061	1.30	1.42	1.55
LL2	.177	.182	.187	4.50	4.62	4.75
LL3	.051	.056	.061	1.30	1.42	1.55
LW1	.108	.113	.118	2.74	2.87	3.00
LW2	.124	.129	.134	3.15	3.28	3.40
LW3	.034	.039	.044	0.86	0.99	1.12
LW4	.124	.129	.134	3.15	3.28	3.40
LW5	.034	.039	.044	0.86	0.99	1.12
LW6	.056	.061	.066	1.42	1.55	1.68
Q1	.019			0.48		
Q2-Q5	.024			0.61		
LS		(.007)			(0.18)	
FW	.009	.014	.019	0.23	0.36	0.48

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TITLE: CASE OUTLINE, LOW VOLTAGE GaN, PowIR-SMD
DRAWING NO. D101028G-WEB
REV C

Pin Description:
Pin 1: Kelvin Source: This pin can be used for the gate return. It is optimized to help the gate drive loop. **Pin 1 and Pin 3** are at the same potential.
Pin 2: Drain: This pin is optimized as a power pin to conduct current between drain and source.
Pin 3: Source: This pin is optimized as a power pin to conduct current between drain and source, it is at the same potential as **Pin 1.**
Pin 4: Gate: The control pin for the device.

Revision history

Document version	Date of release	Description of changes
	02/22/2024	Preliminary datasheet with PPD number (PPD-98011)
Rev A	05/30/2025	Final datasheet with PD number
Rev B	07/30/2025	Updated based on ECN-Z8F80816562
Rev C	04/07/2026	Updated based on ECN-Z8F80915961

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Document reference