



# Getting started with PSOC<sup>™</sup> 4 MCU

## About this document

#### Scope and purpose

This application note introduces you to PSOC<sup>™</sup> 4, an Arm<sup>®</sup> Cortex<sup>®</sup>-M0/M0+ based programmable system-onchip. It helps you explore the PSOC<sup>™</sup> 4 architecture and development tools and explains you how to create your first project using PSOC<sup>™</sup> Creator and ModusToolbox<sup>™</sup>, the development tools for PSOC<sup>™</sup> 4; also guides you to more resources to accelerate in-depth learning about PSOC<sup>™</sup> 4.

#### Intended audience

This application note is intended for engineers new to PSOC<sup>™</sup> and ModusToolbox<sup>™</sup>, and those with experience in working with embedded microcontrollers.

#### Associated part family

All PSOC<sup>™</sup> 4 parts

Software version

PSOC<sup>™</sup> Creator 4.4 SP2 or higher, ModusToolbox<sup>™</sup> 3.2 or higher.

#### More code examples? We heard you.

To access an ever-growing list of PSOC<sup>™</sup> 4 code examples using ModusToolbox<sup>™</sup>, please visit the GitHub site. You can also explore the PSOC<sup>™</sup> video library.



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#### 1 Introduction

## 1 Introduction

PSOC<sup>™</sup> 4 is a true programmable embedded system-on-chip integrating custom analog and digital peripheral functions, memory, and an Arm<sup>®</sup> Cortex<sup>®</sup>-M0 or Cortex<sup>®</sup>-M0+ microcontroller on a single chip. This type of system is different from most mixed-signal embedded systems, which use a combination of a microcontroller unit (MCU) and external analog and digital peripherals. These systems typically require many integrated circuits in addition to the MCU, such as opamps, ADCs, and Application-specific Integrated Circuit (ASICs).

PSOC<sup>™</sup> 4 provides a low-cost alternative to the combination of MCU and external ICs. In addition to reducing overall system cost, the programmable analog and digital subsystems allow great flexibility, in-field tuning of the design, and speedy time to market.

The capacitive touch-sensing feature in PSOC<sup>™</sup> 4, known as CAPSENSE<sup>™</sup>, offers unprecedented signal-to-noise ratio; best-in-class liquid tolerance and a wide variety of sensor types such as buttons, sliders, trackpads, and proximity sensors. PSOC<sup>™</sup> 4 offers a best-in-class current consumption of 150 nA while retaining SRAM, programmable logic, and the ability to wake up from an interrupt. PSOC<sup>™</sup> 4 consumes only 20 nA while maintaining wakeup capability in its non-retention power mode. The PSOC<sup>™</sup> 4 family of devices also contain PSOC<sup>™</sup> 4 Bluetooth<sup>®</sup> LE, which integrates a Bluetooth<sup>®</sup> Low Energy radio system. For more details on PSOC<sup>™</sup> 4 Bluetooth<sup>®</sup> LE, see AN91267.

#### Using this document

The next few pages describe PSOC<sup>™</sup> 4 and the advantages of designing with PSOC<sup>™</sup>, ModusToolbox<sup>™</sup>, and PSOC<sup>™</sup> Creator. Or, you can jump right in and quickly build a simple design in ModusToolbox<sup>™</sup> – go to Getting started with PSOC<sup>™</sup> 4 design. If you are using PSOC<sup>™</sup> Creator – go to My first PSOC<sup>™</sup> 4 design using PSOC<sup>™</sup> Creator.



## 2 Development ecosystem

## 2.1 PSOC<sup>™</sup> resources

The wealth of information available on the Infineon webpage can help you select the right PSOC<sup>™</sup> device and, additionally, integrate the device into your designs efficiently and effectively. The following is an abbreviated list for PSOC<sup>™</sup> 4:

- Overview: PSOC<sup>™</sup> portfolio
- Product selectors: PSOC<sup>™</sup> 4. In addition, PSOC<sup>™</sup> Creator includes a device selection tool.
- Datasheets describe and provide electrical specifications for each family.
- Application notes cover a broad range of topics, from basic to advanced level, and include the following:
  - AN88619: PSOC<sup>™</sup> 4 hardware design considerations
  - AN73854: Introduction to bootloaders
  - AN89610: Arm<sup>°</sup> Cortex<sup>°</sup> code optimization
  - AN86233: PSOC<sup>™</sup> 4 low-power modes and power reduction techniques
  - AN57821: Mixed-signal circuit board layout
  - AN89056: PSOC<sup>™</sup> 4 IEC 60730 class B and IEC 61508 SIL Safety Software Library
  - AN64846: Getting started with CAPSENSE<sup>™</sup>
  - AN85951: PSOC<sup>™</sup> 4 and PSOC<sup>™</sup> 6 MCU CAPSENSE<sup>™</sup> design guide
  - AN239751: Flyback inductive sensing (ISX) design guide
- Code examples demonstrate product features and usage
- Technical reference manuals (TRMs): Provide detailed descriptions of the architecture and registers in each PSOC<sup>™</sup> 4 device family.
- PSOC<sup>™</sup> 4 programming specification provides the information necessary to program PSOC<sup>™</sup> 4 nonvolatile memory.
- Development tools:

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- CY8CKIT-040, CY8CKIT-042, CY8CKIT-044, CY8CKIT-046, CY8CKIT-042-BLE, CY8CKIT-045S, and CY8CKIT-041S-MAX PSOC<sup>™</sup> 4 Pioneer kits are easy-to-use and inexpensive development platforms. These include connectors for Arduino-compatible shields and Digilent Pmod daughter cards.
- CY8CKIT-043, CY8CKIT-145-40XX, CY8CKIT-147, CY8CKIT-149, CY8CPROTO-040T, CY8CPROTO-040T-MS, and CY8CPROTO-041TP are very low-cost prototyping platforms for sampling PSOC<sup>™</sup> 4 devices.
- CY8CKIT-040T is a low-cost evaluation kit showing the low power CAPSENSE<sup>™</sup>, low power wake on touch and liquid tolerant features of the PSOC<sup>™</sup> 4000T device.
- The MiniProg3 or MiniProg4 kit provides an interface for flash programming and debug.
- Integrated Development Environment (IDE): There are two development platforms that can be used for application development with PSOC<sup>™</sup> 4 ModusToolbox<sup>™</sup> and PSOC<sup>™</sup> Creator.
- PSOC<sup>™</sup> 4 CAD libraries provide footprint and schematic support for common tools. IBIS models are also available.
- Training videos are available in Infineon website on a wide range of topics including the PSOC<sup>™</sup> 4101 series
- Infineon community enables connection with fellow PSOC<sup>™</sup> developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated PSOC<sup>™</sup> 4 MCU community.

## 2.2 Firmware/application development

There are two development platforms that you can use for application development with PSOC<sup>™</sup> 4:



ModusToolbox<sup>™</sup>: This software includes configuration tools, low-level drivers, middleware libraries, and other packages that enable you to create MCU and wireless applications. All tools run on Windows, macOS, and Linux. ModusToolbox<sup>™</sup> includes an Eclipse IDE, which provides an integrated flow with all the ModusToolbox<sup>™</sup> tools. Other IDEs such as Visual Studio Code, IAR Embedded Workbench and Arm<sup>®</sup> MDK (µVision) are also supported.

ModusToolbox<sup>™</sup> software supports stand-alone device and middleware configurators. Use the configurators to set the configuration of different blocks in the device and generate code that can be used in firmware development. ModusToolbox<sup>™</sup> supports all PSOC<sup>™</sup> 6 MCU and the latest PSOC<sup>™</sup> 4 MCU devices. Table 1 lists the supported PSOC<sup>™</sup> 4 devices. Infineon recommends you to use ModusToolbox<sup>™</sup> for all application development for supported PSOC<sup>™</sup> 4 devices. For more information, see ModusToolbox<sup>™</sup> tools package user guide.

Table 1	List of PSOC <sup>™</sup> 4 devices supported in ModusToolbox <sup>™</sup>
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Devices <sup>1)</sup>	ModusToolbox™	PSOC <sup>™</sup> Creator
PSOC <sup>™</sup> 4000S, PSOC <sup>™</sup> 4100S, PSOC <sup>™</sup> 4100S Plus, PSOC <sup>™</sup> 4100S Plus 256K	Yes	Yes
PSOC <sup>™</sup> 4100S Max, PSOC <sup>™</sup> 4000T, PSOC <sup>™</sup> 4100T Plus	Yes	No
All other PSOC <sup>™</sup> 4 devices	No	Yes
1) PSOC <sup>™</sup> 4 feature set for complet	e PSOC™ 4 portfolio.	

The libraries and enablement software are available on GitHub.

ModusToolbox<sup>™</sup> tools and resources can also be used in the command line. For more information, see the "ModusToolbox<sup>™</sup> build system" section in the ModusToolbox<sup>™</sup> tools package user guide.

**PSOC<sup>™</sup> Creator:** PSOC<sup>™</sup> Creator is a free Windows-based IDE. It enables concurrent hardware and firmware design of PSOC<sup>™</sup> 3, PSOC<sup>™</sup> 4, PSOC<sup>™</sup> 5LP, and PSOC<sup>™</sup> 6 MCU systems. Applications are created using schematic capture and over 150 pre-verified, production-ready peripheral Components.

## 2.2.1 Installing the ModusToolbox<sup>™</sup> tools package

Refer to the ModusToolbox<sup>™</sup> tools package installation guide for details.

## 2.2.2 Choosing an IDE

Figure 1 helps you to choose an appropriate IDE.





#### Figure 1 Choosing an IDE

ModusToolbox<sup>™</sup> software, the latest-generation toolset, is supported across Windows, Linux, and macOS platforms. ModusToolbox<sup>™</sup> software supports 3rd-party IDEs, including the Eclipse IDE, Visual Studio Code, Arm<sup>®</sup> MDK (µVision), and IAR Embedded Workbench. The tools package includes an implementation for all the supported IDEs. The tools support all PSOC<sup>™</sup> 4s. The associated BSP and library configurators also work on all three host operating systems.





#### Figure 2 ModusToolbox™ environment

Certain features of the PSOC<sup>™</sup> 4, such as UDBs (Universal Digital Blocks) and USB are not supported in ModusToolbox<sup>™</sup> version 2.x and earlier. Newer versions of ModusToolbox<sup>™</sup> support the USB host feature and improve the user experience with true multi-core debug support.

It is recommended to use ModusToolbox<sup>™</sup> if you want to build an IoT application using IoT devices or if you are using a PSOC<sup>™</sup> 4 not supported in PSOC<sup>™</sup> Creator.

PSOC<sup>™</sup> Creator is the long-standing proprietary tool that runs on Windows only. This mature IDE includes a graphical editor that supports schematic based design entry with the help of Components. PSOC<sup>™</sup> Creator supports all PSOC<sup>™</sup> 3, PSOC<sup>™</sup> 4, and PSOC<sup>™</sup> 5LP devices, and a subset of PSOC<sup>™</sup> 4 devices.

Choose PSOC<sup>™</sup> Creator if you are using a graphical editor for design entry and code generation, and if the PSOC<sup>™</sup> MCU that you are planning to use is supported by the IDE.

## 2.2.3 ModusToolbox<sup>™</sup> software

ModusToolbox<sup>™</sup> software is a set of tools and software that enables an immersive development experience for creating converged MCU and wireless systems, and enables you to integrate our devices into your existing development methodology. These include configuration tools, low-level drivers, libraries, and operating system support, most of which are compatible with Linux-, macOS-, and Windows-hosted environments.

Figure 3 shows a high-level view of what is available as part of ModusToolbox<sup>™</sup> software. For a more in-depth overview of the ModusToolbox<sup>™</sup> software, see ModusToolbox<sup>™</sup> tools package user guide.





#### Figure 3 ModusToolbox<sup>™</sup> software

The ModusToolbox<sup>™</sup> tools package installer includes the design configurators and tools, and the build system infrastructure.

The build system infrastructure includes the new project creation wizard that can be run independent of the Eclipse IDE, the make infrastructure, and other tools. This means you choose your compiler, IDE, RTOS, and ecosystem without compromising usability or access to our industry-leading CAPSENSE<sup>™</sup> (Human-Machine Interface), AIROC<sup>™</sup> Wi-Fi and Bluetooth<sup>®</sup>, security, and various other features.

One part of the ModusToolbox<sup>™</sup> ecosystem is run-time software that helps you rapidly develop Wi-Fi and Bluetooth<sup>®</sup> applications using connectivity combo devices. See the ModusToolbox<sup>™</sup> run-time software reference guide for details.

Design configurators are the tools that help you create the configurable code for your BSP/Middleware. Jump to Configurators to know more about it.

All the application-level development flows depend on the provided low-level resources. These include:

- Board support packages (BSP) A BSP is the layer of firmware containing board-specific drivers and other functions. The BSP is a set of libraries that provides APIs to initialize the board and access to board level peripherals. It includes low-level resources such as peripheral driver library (PDL) for PSOC<sup>™</sup> 4 and has macros for board peripherals. Custom BSPs can be created to enable support for end-application boards. See BSP Assistant to create your BSP.
- PSOC<sup>™</sup> 4 peripheral driver library (PDL) The PDL integrates device header files, start-up code, and peripheral drivers into a single package. The PDL supports the PSOC<sup>™</sup> 4 family. The drivers abstract the hardware functions into a set of easy-to-use APIs. These are fully documented in the PDL API Reference.

The PDL reduces the need to understand register usage and bit structures, thus easing software development for the extensive set of peripherals in the PSOC<sup>™</sup> 4 series. You configure the driver for your application, and then use API calls to initialize and use the peripheral.

 Middleware (MW) – Extensive middleware libraries that provide specific capabilities to an application. The available middleware spans across connectivity (OTA, Bluetooth<sup>®</sup>, AWS IoT, Bluetooth<sup>®</sup> LE, Secure Sockets) to PSOC<sup>™</sup> 4-specific functionality (CAPSENSE<sup>™</sup>, USB, device firmware upgrade (DFU), emWin). All the middleware is delivered as libraries and via GitHub repositories.



## 2.2.4 ModusToolbox<sup>™</sup> applications

With the release of ModusToolbox<sup>™</sup> v3.x, multi-core support is introduced, which has altered the folder structure slightly from the previous version of ModusToolbox<sup>™</sup>, but PSOC<sup>™</sup> 4 has single core only.



#### Figure 4 Application type

The following shows the new folder structure for an example single-core application:



```
<root>
  ApplicationName
  ->Makefile (MTB TYPE=COMBINED)
  ->deps
      lib1.mtb (local)
      lib2.mtb (shared)
  ->libs
      lib1 (Infineon Git repo)
  ->bsps
      TARGET BSP1 (not an Infineon Git repo; completely app-owned)
  ->templates
      TARGET BSP1
        design.modus
        design.capsense
  ->main.c
  ->helper.h
  ->helper.c
  mtb shared
    lib2/... (Infineon Git repo)
```

Figure 5 Folder structure for single-core applications

## 2.2.5 PSOC<sup>™</sup> 4 software resources

The software for PSOC<sup>™</sup> 4s includes configurators, drivers, libraries, middleware, as well as various utilities, makefiles, and scripts. It also includes relevant drivers, middleware, and examples for use with IoT devices and connectivity solutions. You can use any or all tools in any environment you prefer.

## 2.2.5.1 Configurators

ModusToolbox<sup>™</sup> software provides graphical applications called configurators that make it easier to configure a hardware block. For example, instead of having to search through all the documentation to configure a serial communication block as a UART with a desired configuration, open the appropriate configurator and set the baud rate, parity, and stop bits. Upon saving the hardware configuration, the tool generates the "C" code to initialize the hardware with the desired configuration.

There are two types of configurators: BSP configurators that configure items that are specific to the MCU hardware and library configurators that configure options for middleware libraries.

Configurators are independent of each other, but they can be used together to provide flexible configuration options. They can be used stand alone, in conjunction with other tools, or within a complete IDE. Configurators are used for:

- Setting options and generating code to configure drivers
- Setting up connections such as pins and clocks for a peripheral
- Setting options and generating code to configure middleware

For PSOC<sup>™</sup> 4 applications, the available Configurators include:

• Device Configurator: Sets up the system (platform) functions and the basic peripherals (for example, UART, Timer, PWM).



- CAPSENSE<sup>™</sup> Configurator and Tuner: Configures CAPSENSE<sup>™</sup> and generates the required code.
- Smart I/O Configurator: Configures the Smart I/O.

Each of the above configurators create their own files (For example, design.cycapsense for CAPSENSE<sup>™</sup>). BSP configurator files (For example, design.modus or design.cycapsense) are provided as part of the BSP with default configurations while library configurators (e.g. design.cybt) are provided by the application. When an application is created based on Infineon BSP, the application makes use of BSP configurator files from the Infineon BSP repo. You can customize/create all the configurator files as per your application requirement using ModusToolbox<sup>™</sup> software. See BSP Assistant to create your custom BSP. See ModusToolbox<sup>™</sup> help for more details.

## 2.2.5.2 Library management for PSOC<sup>™</sup> 4

The application can have shared/local libraries for the projects. If needed, different projects can use different versions of the same library. The shared libraries are downloaded under the mtb\_shared directory. The application should use the deps folder to add library dependencies. The deps folder contains files with the .mtb file extension, which is used by ModusToolbox<sup>™</sup> to download its git repository. These libraries are direct dependencies of the ModusToolbox<sup>™</sup> project.

The Library Manager helps to add/remove/update the libraries of your projects. It also identifies whether particular library has a direct dependency on any other library using the manifest repository available on GitHub, and fetches all its dependencies. These dependency libraries are indirect dependencies of the ModusToolbox<sup>™</sup> project. These dependencies can be seen under the libs folder. For more information, see the Library Manager user guide located at <install\_dir> /ModusToolbox/tools\_<version>/library-manager/docs/ library-manager.pdf.

## 2.2.5.3 Software development for PSOC<sup>™</sup> 4

The ModusToolbox<sup>™</sup> ecosystem provides significant source code and tools to enable software development for PSOC<sup>™</sup> 4s. You use tools to:

- Specify how you want to configure the hardware.
- Generate code for that purpose, which you use in your firmware.
- Include various middleware libraries for additional functionality, like Bluetooth<sup>®</sup> LE connectivity or FreeRTOS.

This source code makes it easier to develop the firmware for supported devices. It helps you quickly customize and build firmware without the need to understand the register set.

In the ModusToolbox<sup>™</sup> environment, you use configurators to configure either the device, or a middleware library, like the Bluetooth<sup>®</sup> LE stack or CAPSENSE<sup>™</sup>. The BSP configurator files are used to configure device peripherals, pins, and memory using peripheral driver library code. The middleware is delivered as separate libraries for each feature/function such that it can be used across multiple platforms. For example, abstractionrtos, lwip, usb, etc.

Firmware developers who wish to work at the register level should refer to the driver source code from the PDL. The PDL includes all the device-specific header files and startup code you need for your project. It also serves as a reference for each driver. Because the PDL is provided as source code, you can see how it accesses the hardware at the register level.

Some devices do not support particular peripherals. The PDL is a superset of all the drivers for any supported device. This superset design means:

- All API elements needed to initialize, configure, and use a peripheral are available.
- The PDL is useful across various PSOC<sup>™</sup> 4s, regardless of available peripherals.
- The PDL includes error checking to ensure that the targeted peripheral is present on the selected device.



This enables the code to maintain compatibility across products of the PSOC<sup>™</sup> 4 family, as long as the peripherals are available. A device header file specifies the peripherals that are available for a device. If you write code that attempts to use an unsupported peripheral, you will get an error at compile time. Before writing code to use a peripheral, consult the datasheet for the particular device to confirm support for that peripheral.

As the following figure shows, with the ModusToolbox  $^{\scriptscriptstyle \rm M}$  software, you can:

- **1.** Choose a BSP (Project Creator).
- **2.** Create a new application based on a list of starter applications, filtered by the BSPs that each application supports (Project Creator).
- 3. Add BSP or middleware libraries (Library Manager).
- **4.** Develop your application firmware using PDL for PSOC<sup>™</sup> 4 (IDE of choice or command line).

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> AIROC <sup>™</sup> Bluetooth® BSPs				enables you to evaluate and develop with	Cashar Elbara barak		
> AIROC <sup>™</sup> Connectivity BSPs				Cypress's fifth-generation, low-power	enter inter text	Browse for Application y g and a g and	reating applications using
✓ PMG BSPS ✓ PSOC™ 4 BSPs				CAPSENSE™ solution using the PSOC™ 4000T	Template Application	New Application Name New BSP Name	
CY8CKIT-040T C	CV8C4046LQI-T452 <none></none>			device.	<ul> <li>Getting Started</li> </ul>	For more details, see the <u>README on GitHub</u> .	
CY8CKIT-041-41XX C	CY8C4146AZI-S433 <none></none>			Kit Features:	Hello World	Hello_wond APP_CTOCPROTO-0	
CY8CKIT-041S-MAX C	CY8C4149AZI-5598 < none> CV8C4548A7L5485 < none>			World's Most Reliable Lowest Power	Power Modes		
CY8CKIT-145-40XX C	CY8C4045AZI-S413 <none></none>			CAPSENSE <sup>™</sup> Solution	✓ Peripherals		
CY8CKIT-149 C	CY8C4147AZI-S475 <none></none>			On-board Programmer and Debugger	Emulated EEPROM     GBIO Interrupt		
CY8CPROTO-040T C	CV8C4046LQI-T452 <none></none>			Kit Contents:	GPIO Pins		
CY8CPROTO-041TP C	CY8C4147AZQ-T495 <none></none>		-		I2C Master EzI2C Slave	Designed Charles	
KIT_PSOC4+HVMS-128K_LITE C	CY8C4147LWE+HVS135X <none></none>			CY8CPROID-0401 PSOC <sup>®</sup> 40001     CAPSENSE <sup>®</sup> Prototyning Kit	I2C Slave Using Callbacks	Browse Starter	
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> PSOC™ 6 BSPs					SPI Slave		
> PSOC <sup>™</sup> Control BSPs					TCPWM event counter		
Reference Derion RSRr		Cho	oose Board Supp	ort	CPWW square wave		
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			гаскаде		Summary:		
					BSP: CY8CPROTO-040T		
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ess "Next" to select application.				I			
				Next > Close		< Back	Create Close
					4		
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Enter filter text	Uodati	Available Remove	Properties README.md RELI	Browse	Image: Nonje X     100 Debu     1111 Regi     100 Perip     Image: Nonje X       > 100     Hello_World       > 100     mtb_shared	Maint X     System entrance point. This function performs     - initial setup of device     - configure the SCB block as RBAT interface     - source our Stable block as RBAT interface	Dutine ×     B: Outine ×     B: ½ № ½ ●     Gypdlh     Gypph
Enter filter text	Updat	Available Remove	Properties README.md RELI	Browse	Image: A constraint of the cons	[2] maint X + System extrance point. This function performs + - initial setup of device + - configure the SS block as UAX interface + - points out "Mollo World" via UAX interface + - Blinds and US2 under finance control 1 if in	D      Contine X
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ModusToolbox<sup>™</sup> resources and middleware

## 2.2.6 ModusToolbox<sup>™</sup> help

The ModusToolbox<sup>™</sup> ecosystem provides documentation and training. One way to access it is launching the Eclipse IDE for ModusToolbox<sup>™</sup> software and navigating to the following **Help** menu items:

Choose **Help** > **ModusToolbox**<sup>™</sup> **General Documentation**:

- **ModusToolbox™ Documentation Index:** Provides brief descriptions and links to various types of documentation included as part the ModusToolbox<sup>™</sup> software.
- **ModusToolbox<sup>™</sup> Installation Guide:** Provides instructions for installing the ModusToolbox<sup>™</sup> software.



- **ModusToolbox™ User Guide:** This guide primarily covers the ModusToolbox<sup>™</sup> aspects of building, programming and debugging applications. It also covers various aspects of the tools installed along with the IDE.
- **ModusToolbox™ Training Material:** Links to the training material available at https://github.com/Infineon/training-modustoolbox.
- Release Notes

For documentation on Eclipse IDE for ModusToolbox<sup>™</sup>, choose **Help** > **Eclipse IDE for ModusToolbox<sup>™</sup> Documentation**:

- **User Guide:** Provides descriptions about creating applications as well as building, programming, and debugging them using Eclipse IDE
- Eclipse IDE Survival Guide

## 2.3 Support for other IDEs

You can develop firmware for PSOC<sup>™</sup> 4s using your preferred IDE such as Eclipse IDE, IAR Embedded Workbench, Keil µVision 5, or Visual Studio Code.

ModusToolbox<sup>™</sup> Configurators are stand-alone tools that can be used to set up and configure PSOC<sup>™</sup> 4 resources and other middleware components without using the Eclipse IDE. The Device Configurator and middleware configurators use the design.x files within the application workspace. You can then point to the generated source code and continue developing firmware in your IDE.

If there is a change in the device configuration, edit the design.x files using the configurators and regenerate the code. It is recommended that you generate resource configurations using the configuration tools provided with ModusToolbox<sup>™</sup> software.

See ModusToolbox<sup>™</sup> tools package user guide for details.

## 2.4 PSOC<sup>™</sup> Creator

PSOC<sup>™</sup> Creator is an IDE that enables concurrent hardware and firmware editing, compiling, and debugging of PSOC<sup>™</sup> systems. Do the following to browse through PSOC<sup>™</sup> Creator, as shown in Figure 7:

- **1.** Drag and drop Components to build your hardware system design
- 2. Co-design your application firmware with the PSOC<sup>™</sup> hardware
- **3.** Configure Components with config tools
- 4. Explore the library of more than 100 Components
- 5. Review Component datasheets





Figure 7

Features of PSOC<sup>™</sup> Creator features

## 2.4.1 PSOC<sup>™</sup> Creator help

Download the PSOC<sup>™</sup> Creator's latest version from the PSOC<sup>™</sup> Creator home page, launch the PSOC<sup>™</sup> Creator, and navigate to the following:

- Quick Start Guide: Choose Help > Documentation > Quick Start Guide. This guide gives you the basics for developing PSOC<sup>™</sup> Creator projects.
- Simple Component example projects: Choose File > Open > Example projects. These example projects demonstrate how to configure and use PSOC<sup>™</sup> Creator Components.
- System Reference Guide: Choose Help > System Reference > System Reference Guide. This guide lists and describes the system functions provided by PSOC<sup>™</sup> Creator.
- Component datasheets: Right-click a Component and select Open Datasheet. Visit the PSOC<sup>™</sup> 4 Component datasheets page for a list of all PSOC<sup>™</sup> 4 Component datasheets.
- PSOC<sup>™</sup> Creator training videos: These videos provide step-by-step instructions on how to get started with PSOC<sup>™</sup> Creator.
- Document Manager: PSOC<sup>™</sup> Creator provides a document manager to help you to find and review document resources easily. To open the document manager, choose the menu item Help > Document Manager.

## 2.5 Technical support

If you have any questions, our technical support team is happy to assist you. You can create a support request on the Technical support page. The support team monitors and responds to your questions, issues, and bug reports posted on the GitHub repositories.



## **3** PSOC<sup>™</sup> 4 feature set

PSOC<sup>™</sup> 4 has an extensive set of features, which include a CPU and memory subsystem, a digital subsystem, an analog subsystem, and system resources, as shown in Figure 8. The following sections describe each feature. For more information, see the PSOC<sup>™</sup> 4 family device datasheets, technical reference manuals (TRMs), and application notes listed in PSOC<sup>™</sup> resources.



#### Figure 8

#### PSOC<sup>™</sup> 4000T architecture

The PSOC<sup>™</sup> 4 portfolio consists of several families of Arm<sup>®</sup> CM0 and CM0+ microcontrollers. Most devices in the portfolio have CAPSENSE<sup>™</sup> technology for capacitive-sensing applications. Other key features of the PSOC<sup>™</sup> 4 portfolio include a customizable analog front end through programmable analog blocks and wired and wireless connectivity options such as USB, Controller Area Network (CAN), and Bluetooth<sup>®</sup> LE. These unique features make PSOC<sup>™</sup> 4 the industry's most flexible and scalable low-power mixed-signal architecture. The PSOC<sup>™</sup> 4 devices are classified as different families, as shown in Table 2, based on different features.



#### Table 2PSOC<sup>™</sup> 4 families

Classification	Family	Features	Details
Entry level	PSOC <sup>™</sup> 4000 family	CAPSENSE <sup>™</sup>	Table 3
Intelligent analog	PSOC <sup>™</sup> 4100 family	CAPSENSE <sup>™</sup> + Programmable Analog	Table 4
Programmable digital	PSOC <sup>™</sup> 4200 family	CAPSENSE <sup>™</sup> + Programmable Analog + Programmable Digital Blocks	Table 5
Application specific	PSOC <sup>™</sup> 4500 family	CAPSENSE <sup>™</sup> + Motor Control	Table 6
	PSOC <sup>™</sup> 4700 family	CAPSENSE <sup>™</sup> + Inductive Sensing	
Analog coprocessor <sup>1)</sup>	PSOC <sup>™</sup> 4A00 family	CAPSENSE <sup>™</sup> + Programmable Analog Blocks	AN211293

**Note:** In Table 3 and Table 4, the columns highlighted in green indicate that the device family is supported in ModusToolbox<sup>™</sup>.

#### Table 3PSOC™ 4000 family features

Features		PSOC <sup>™</sup> 4000	PSOC <sup>™</sup> 4000S	PSOC <sup>™</sup> 4000T
CPU		16-MHz Cortex <sup>®</sup> -M0	48-MHz Cortex <sup>®</sup> -M0+	48-MHz Cortex <sup>®</sup> -M0+
Flash memory		16 KB	32 KB	64 KB
SRAM		2 KB	4 KB	8 KB
GPIOs		20	36	21
CAPSENSE™	Sense pins	16	35	19
	Ultra-Low Power Wake on Touch (WoT)	No	No	Yes
	CAPSENSE <sup>™</sup> IP Generation	Fourth-generation	Fifth-generation	Fifth-generation Low Power
Single-slope ADC (10-bit 46-	ksps)	None	1	None
Comparators		1 CSD comparator with a fixed threshold (1.2 V)	Two low-power comparators with wakeup feature	None
IDACs <sup>1)</sup>		One 7-bit and one 8-bit	Two 7-bits	None
Smart I/O ports		None	2	None

(table continues...)



Table 3	(continued) PSOC <sup>™</sup> 4000 f	amily features		
Features		PSOC <sup>™</sup> 4000	PSOC™ 4000S	PSOC™ 4000T
Power supp	oly range	1.71 V to 5.5 V	1.71 V to 5.5 V	1.71 V to 5.5 V
Low-power	modes	Deep Sleep at 2.5 μΑ	Deep Sleep at 2.5 μA	Deep Sleep at 2.5 µA
Segment LC	CD drive	None	4 COM segment LCD drive	None
Serial comr	nunication	One I2C	Two SCBs with programmable I2C, SPI, or UART	1 SCB with programmable I2C, SPI, or UART. 1 SCB having I <sup>2</sup> C only
Timer Coun (TCPWM)	ter Pulse-Width Modulator	1	5	2
Clocks	Internal main oscillator (IMO)	24 MHz/32 MHz	24 MHz to 48 MHz	24 MHz to 48 MHz
	Internal low-speed oscillator (ILO)	32-kHz internal ILO	40 kHz	40 kHz
	Watch crystal oscillator (WCO)	None	32-kHZ	None
Power supp	oly monitoring	Power-on reset (POR)Brown-out detection (BOD)	POR, BOD	POR, BOD
Supported	kit	CY8CKIT-040 pioneer kit	-	CY8CKIT-040T PSOC <sup>™</sup> 4000T CAPSENSE <sup>™</sup> Evaluation Kit, CY8CPROTO-040T PSOC <sup>™</sup> 4000T CAPSENSE <sup>™</sup> Prototyping Kit, and CY8CPROTO-040T- MS Multi-Sense Prototyping Kit
Supported	IDE	PSOC <sup>™</sup> Creator	PSOC <sup>™</sup> Creator, ModusToolbox <sup>™</sup>	ModusToolbox™

1) IDACs are available only when CAPSENSE<sup>™</sup> is not in use. See the respective PSOC<sup>™</sup> 4 architecture TRM for more details.

Table 4	PSOC <sup>™</sup> 41	00 family featu	Ires						
Features	PSOC™	PSOC"	PSOC"	PSOC™	PSOC <sup>™</sup>	PSOC™	PSOC™	PSOC <sup>™</sup>	PSOC"
	4100	4100S	4100S Plus	4100S Plus 256K	4100PS	4100M	4100 BL <sup>1)</sup>	4100S Max	4100T Plus
CPU	24-MHz Cortex <sup>®</sup> - M0	48-MHz Cortex <sup>®</sup> -M0+	48-MHz Cortex <sup>°</sup> -M0+	48-MHz Cortex <sup>°</sup> -M0+	48-MHz Cortex <sup>°</sup> - M0+	24-MHz Cortex <sup>®</sup> - M0	24-MHz Cortex <sup>®</sup> - M0	48-MHz Cortex <sup>®</sup> -M0+	48-MHz Cortex <sup>®</sup> -M0+
DMA	N/A	N/A	8 channels	8 channels	8 channels	8 channels	8 channels	16 channels	8 channels
Flash memory	32 KB	64 KB	128 KB	256 KB	32 KB	128 KB	256 KB	384 KB	128 KB
SRAM	4 KB	8 KB	16 KB	32 KB	4 KB	16 KB	32 kB	32 KB	32 KB
GPIOS	36	36	54	54	38	55	36	84	53
CAPSENSE		1 channel,	1 channel,	1 channel,	1 channel,	2		2 channels,	1 channel,
	channel, 35	35 sensors	53 sensors	53 sensors	33 sensors	channels	channel, 25	80 sensors	32 sensors
	sensors					54 Sansors	sensors	(az collitiot mux)	
	_					CINCIDO			
12-bit SAR ADC with sequencer	806- KSPS	1-MSPS	1-MSPS	1-MSPS	1-MSPS	806- KSPS	806- KSPS	1-MSPS	1-MSPS
Opamps (programmable)	2	2	2	2	4/PGA	4	2	2	None
Programmable Voltage Reference (PVref)	None	None	None	None	Four channels	None	None	None	None
Voltage DAC (VDAC)	None	None	None	None	Two 13-bit VDAC	None	None	None	None
Comparators (low power with wakeup feature)	5	7	7	2	2	5	2	2	None
(table continues,	_								

## Getting started with PSOC<sup>™</sup> 4 MCU

3 PSOC<sup>™</sup> 4 feature set



Table 4		(continue	d) PSOC <sup>TM</sup> 4100	family feature:	S					
Feature	S	PSOC™	PSOC <sup>™</sup>	PSOC"	PSOC <sup>™</sup>	PSOC"	PSOC™	PSOC™	PSOC <sup>™</sup>	PSOC"
		4100	4100S	4100S Plus	4100S Plus 256K	4100PS	4100M	4100 BL <sup>1)</sup>	4100S Max	4100T Plus
IDACs <sup>2)</sup>		One 7-bit and one 8-bit	Two 7-bits	Two 7-bits	Two 7-bits	Two 7-bits	Two 7- bits and two 8- bits	One 7- bit and one 8-bit	None	None
Smart I/	0 ports	None	2	3	2	1	None	None	3	1
Power sur	npply	1.71 V to 5.5 V	1.71 V to 5.5 V	1.71 V to 5.5 V	1.71 V to 5.5 V	1.71 V to 2.5 μΑ	1.71 V to 5.5 V	1.71 V to 5.5 V	1.71 V to 5.5 V	1.71 V to 5.5 V
Low- power	Deepslee p	1.3 µA	2.5 µА	2.5 µА	2.5 µА	2.5 µA	1.35 µA	2.5 µA	2.5 µA	2.5 µА
modes	Hibernat e	150 nA	NA	NA	NA	NA	150 nA	NA	NA	None
	Stop	20 nA	NA	NA	NA	NA	35 nA	NA	NA	None
Segmen drive	t LCD	4 COM	4 COM	4 COM	4 COM	4 COM	4 COM	4 COM	4 COM	None
SCBs wi program I2C, SPI,	th imable or UART	2	ĸ	ъ	5	£	4	2	5	5 (2 SCB, 3 UART)
TCPWM		4	5	8	8	8	8	4	8	6
CAN		None	None	1	None	None	None	None	1	None
BLE		None	None	None	None	None	None	4.1/4.2	None	None
Clocks	OMI	3 MHz to 24 MHz	24 MHz to 48 MHz	24 MHz to 48 MHz	24 MHz to 48 MHz	24 MHz to 48 MHz	3 MHz to 48 MHz	24 MHz to 48 MHz	24 MHz to 48 MHz	24 MHz to 48 MHz
	ILO	32 kHz	40 kHz	40 kHz	40 kHz	40 kHz	32 kHz	40 kHz	40 kHz	40 kHz
	WCO	Nil	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz
(table c	ontinues									

## Getting started with PSOC<sup>™</sup> 4 MCU

3 PSOC<sup>™</sup> 4 feature set

Application note



Table 4	(continue	d) PSOC <sup>™</sup> 4100	family feature:	S					
Features	PSOC™ 4100	PSOC™ 4100S	PSOC™ 4100S Plus	PSOC™ 4100S Plus 256K	PSOC™ 4100PS	PSOC <sup>TM</sup> 4100M	PSOC <sup>TM</sup> 4100 BL <sup>1)</sup>	PSOC™ 4100S Max	PSOC™ 4100T Plus
Power supply monitoring	POR, BOD, Low- voltage detectio n (LVD)	POR, BOD	POR, BOD	POR, BOD	POR, BOD	POR, BOD, LVD	POR, BOD, LVD	POR, BOD	POR, BOD
Supported kit	1	ı	CY8CKIT-149 prototyping kit	ı	CY8CKIT-14 7 prototypin g kit	CY8CKIT- 044 pioneer kit	CY8CKIT- 042 BLE pioneer kit	CY8CKIT-041S -MAX pioneer kit	PSOC <sup>™</sup> 4100T Plus CAPSENSE <sup>™</sup> prototyping kit
Supported IDE	PSOC <sup>TM</sup> Creator	PSOC™ Creator, ModusToolbo X™	PSOC™ Creator, ModusToolbo X™	PSOC™ Creator, ModusToolbo X™	PSOC™ Creator	PSOC™ Creator	PSOC™ Creator	ModusToolbo X <sup>™</sup>	ModusToolbox
<ol> <li>See AN91267 for</li> <li>IDACs are availab</li> </ol>	getting started	d with PSOC™ 4 Blue CAPSENSE™ is not i	etooth <sup>®</sup> LE Family d n use. See the resp	levices. ective PSOC™ 4 arcl	itecture TRM m	ore details.			

Getting started with PSOC<sup>™</sup> 4 MCU







Table 5	P	SOC <sup>™</sup> 4200 family	features			
Features		PSOC <sup>™</sup> 4200	PSOC <sup>™</sup> 4200DS	PSOC <sup>™</sup> 4200M	PSOC™ 4200L	PSOC <sup>™</sup> 4200 BL <sup>1)</sup>
CM0 CPU		48 MHz Cortex <sup>®</sup> - M0				
DMA		None	8 channels	8 channels	32 channels	None
Flash mem	ory	32 KB	64 KB	128 KB	256 KB	256 KB
SRAM		4 KB	8 KB	16 KB	32 KB	32 KB
GPIOs		36	21	55	96	36
CAPSENSE	тм	1 channel, 35 sensors	None	2 channels, 54 sensors	2 channels, 94 sensors	1 channel, 35 sensors
ADC (12-bi SAR ADC w sequencer	t, 1-MSPS ith )	1	None	1	1	1
Opamps (programn	nable)	2	None	2	4	2
Comparato power with feature)	ors (low 1 wakeup	2	2	2	2	2
IDACs <sup>2)</sup>		One 7-bits and one 8-bit	None	Two 7-bits and two 8-bits	Two 7-bits and two 8-bits	One 7-bit and one 8-bit
Programm blocks (UD	able logic Bs)	4	4	4	8	4
Smart I/O ports		None	1	None	None	None
Power supply range		1.71 V to 5.5 V				
Low- power	Deep Sleep	1.3 µA	2 μΑ	1.3 µA	1.3 µA	1.5 µA
Low- power modes	Hibernat e	150 nA	NA	150 nA	150 nA	150 nA
	Stop	20 nA	NA	20 nA	20 nA	20 nA
Segment L	CD drive	4 COM	None	4 COM	8 COM	4 COM
SCBs with programm SPI, or UAF	able I2C, RT	2	3	4	4	2
TCPWM		4	4	8	8	4
CAN		None	None	2	2	None
BLE		None	None	None	None	4.1/4.2
USB Full S Device Cor (USB)	beed Itroller	None	None	None	Yes	None

(table continues...)



Table 5	(c	ontinued) PSOC™	4200 family feat	ures		
Features		PSOC <sup>™</sup> 4200	PSOC <sup>™</sup> 4200DS	PSOC <sup>™</sup> 4200M	PSOC <sup>™</sup> 4200L	PSOC <sup>™</sup> 4200 BL <sup>1)</sup>
Clocks	IMO	3 MHz to 48 MHz	3 MHz to 48 MHz	3 MHz to 48 MHz	3 MHz to 48 MHz	3 MHz to 48 MHz
	ILO	32 kHz	40 kHz	32 kHz	32 kHz	32 kHz
	WCO	None	None	32 kHz	32 kHz	32 kHz
	External crystal oscillator (ECO)	None	None	4 MHz to 33 MHz	None	None
Power sup monitoring	ply g	POR, BOD, LVD	POR, BOD	POR, BOD, LVD	POR, BOD, LVD	POR, BOD, LVD
Supported kit		CY8CKIT-042 pioneer kit	CY8CKIT-146 prototyping kit	CY8CKIT-044 pioneer kit	CY8CKIT-046 pioneer kit	CY8CKIT-042 Bluetooth <sup>®</sup> LE pioneer kit
Supported	IDE	PSOC <sup>™</sup> Creator	PSOC <sup>™</sup> Creator	PSOC <sup>™</sup> Creator	PSOC <sup>™</sup> Creator	PSOC <sup>™</sup> Creator

1) See AN91267 for getting started with PSOC<sup>™</sup> 4 Bluetooth<sup>®</sup> LE family devices.

2) IDACs are available only when CAPSENSE<sup>™</sup> is not in use. See the respective PSOC<sup>™</sup> 4 architecture TRM for more details.

#### Table 6 PSOC<sup>™</sup> 4500 and PSOC<sup>™</sup> 4700 family features

Features		PSOC <sup>™</sup> 4500S	PSOC <sup>™</sup> 4700S	
CM0+ CPU		48 MHz Cortex <sup>®</sup> -M0+	48 MHz Cortex <sup>®</sup> -M0+	
DMA		8 channels	None	
Flash memory		256 KB	32 KB	
SRAM		32 KB	4 KB	
GPIOs		53	36	
CAPSENSE™		1 channel, 52 sensors	1 channel, 35 sensors	
MagSense		None	1 channel	
ADC		Two 12-bits, 1-MSPS SAR ADCs with sequencer	10-bit, 16.8-ksps Single slope ADC	
Opamps (programmable)	)	4	None	
Comparators (low power	with wakeup feature)	2	2	
IDACs <sup>1)</sup>		Two 7-bits	Two 7-bits	
Smart I/O ports		2	2	
Power supply range		1.71 V to 5.5 V	1.71 V to 5.5 V	
Low-power modes	Deep Sleep	1.3 µA	2.5 μΑ	
	Hibernate	150 nA	NA	
	Stop	20 nA	NA	
Segment LCD drive	· ·	4 COM	8 COM	

(table continues...)



Table 6	(continued) PSOC <sup>™</sup> 4500 and	d PSOC™ 4700 family features		
Features		PSOC™ 4500S	PSOC™ 4700S	
SCBs with programmable I2C, SPI, or UART		5	2	
ТСРѠМ		8	5	
Motor Control Acceleration (MCA)		2	None	
Clocks	IMO	24 MHz to 48 MHz	24 MHz to 48 MHz	
	ILO	40 kHz	40 kHz	
	WCO	32 kHz	32 kHz	
	ECO	4 MHz to 33 MHz	None	
Power supply m	onitoring	POR, BOD	POR, BOD	
Supported kit		CY8CKIT-045S pioneer kit	CY8CKIT-148 evaluation kit	
Supported IDE		PSOC <sup>™</sup> Creator	PSOC <sup>™</sup> Creator	

1) IDACs are available only when CAPSENSE<sup>™</sup> is not in use. See the respective PSOC<sup>™</sup> 4 architecture TRM for more details.



#### 4 PSOC<sup>™</sup> is more than an MCU

## 4 PSOC<sup>™</sup> is more than an MCU

**Figure 9** shows that a typical MCU contains a CPU (such as 8051 or an Arm<sup>®</sup> Cortex<sup>®</sup>) with a set of peripheral functions such as ADCs, DACs, UARTs, SPIs, and general I/O, all linked to the CPU's register interface. Within the MCU, the CPU is the "heart" of the device – the CPU manages everything from setup to data movement to timing. Without the CPU, the MCU cannot function.

Figure 10 shows that PSOC<sup>™</sup> is quite different. With PSOC<sup>™</sup>, the CPU, analog, digital, and I/O are equally important resources in a programmable system. It is the system's interconnect and programmability that is the heart of PSOC<sup>™</sup> – not the CPU. The peripheral analog and digital are interconnected with a highly configurable matrix of signal and data bus meshing that allows you to create custom designs that meet your application requirements. You can program PSOC<sup>™</sup> to emulate an MCU, but you cannot program an MCU to emulate PSOC<sup>™</sup>.



#### Figure 9

Typical MCU block diagram



#### Figure 10

PSOC<sup>™</sup> block diagram

A typical MCU requires CPU firmware to process state machines, use a timer for timing, and drive an output pin. Therefore, the functional path is always through the CPU. However, with PSOC<sup>™</sup>, asynchronous parallel processing is possible. You can configure a PSOC<sup>™</sup> to have elements that operate independently from the CPU. The projects included with this application note demonstrate this concept. The PSOC<sup>™</sup> is configured to make an LED blink without writing any code for the CPU as mentioned in section Part 1: Create the design.



#### 4 PSOC<sup>™</sup> is more than an MCU

## 4.1 The concept of PSOC<sup>™</sup> Creator Components

One other important thing about PSOC<sup>™</sup> is the availability of PSOC<sup>™</sup> Creator IDE. In PSOC<sup>™</sup> Creator, different PSOC<sup>™</sup> resources are organized as graphical elements called Components, which can be dragged and dropped onto a schematic to quickly build designs. Every peripheral in PSOC<sup>™</sup> is available as a pre-validated PSOC<sup>™</sup> Creator Component – PWM Component, ADC Component, DAC Component, CAPSENSE<sup>™</sup> Component, UART Component and so on. The availability of pre-validated Components in the PSOC<sup>™</sup> Creator significantly reduces the development time. It also allows you to quickly make changes in the design using graphical options.

For example, configuring a PWM to blink an LED in a typical microcontroller involves the following:

- **1.** Locate the registers corresponding to the PWM block.
- 2. Calculate the values to be written to the PWM registers based on the required PWM period and duty cycle.
- **3.** Write many lines of code to configure the PWM registers, set the pin drive mode, and to connect the PWM output to the pin. Many MCUs do not offer alternate pins to connect to the internal blocks.

To implement the same functionality in PSOC<sup>™</sup> is a trivial exercise, as you will find out later in this application note. Later, if you need to reconfigure the same PWM block to a Timer, you do not need anything more than a few mouse clicks in PSOC<sup>™</sup> Creator.

The PSOC<sup>™</sup> also has programmable digital blocks known as Universal Digital Blocks (UDBs). PSOC<sup>™</sup> Creator also provides several Components made of UDBs such as UART, SPI, I2C, Timer, PWM, Counter, Digital Gates (AND, OR, NOT, XOR, and so on), and many more. You can even create your own custom state machines and digital logic using the UDBs in PSOC<sup>™</sup> Creator. The method to create your own custom PSOC<sup>™</sup> Creator Components is provided in the PSOC<sup>™</sup> Creator Component author guide.



## Getting started with PSOC<sup>™</sup> 4 design

This section provides the following:

5

- Demonstrate how to build a simple PSOC<sup>™</sup> 4-based design and program it on to the development kit
- Makes it easy to learn PSOC<sup>™</sup> 4 design techniques and how to use the ModusToolbox<sup>™</sup> software with different IDEs.

**Note**: You can use any supported IDE, but this section uses the Eclipse IDE as an example.

## 5.1 Prerequisites

Before you get started, make sure that you have the appropriate development kit for your PSOC<sup>™</sup> 4 product line and have installed the required software. You also need internet to access the GitHub repositories during project creation.

#### 5.1.1 Hardware

Testing this design requires one of the kits listed in Table 7, which has an integrated programmer.

Kit name	Kit type	Supported device family	Part number				
CY8CKIT-145	Prototyping kit	PSOC <sup>™</sup> 4000S	CY8C4045AZI-S413				
CY8CKIT-149	Prototyping kit	PSOC <sup>™</sup> 4100S Plus	CY8C4147AZI-S475				
CY8CKIT-041S-Max	Pioneer kit	PSOC <sup>™</sup> 4100S Max	CY8C4149AZI-S598				
CY8CKIT-040T	Evaluation kit	PSOC <sup>™</sup> 4000T	CY8C4046LQI-T452				
CY8CPROTO-040T	Prototyping kit	PSOC <sup>™</sup> 4000T	CY8C4046LQI-T452				
CY8CPROTO-041TP	Prototyping kit	PSOC <sup>™</sup> 4100T Plus	CY8C4147AZQ-T495				
CY8CPROTO-040T-MS	Prototyping kit	PSOC <sup>™</sup> 4000T	CY8C4046LQI-T452				

Table 7 List of PSOC<sup>™</sup> 4 pioneer kits, prototyping kits, and supported devices

## 5.1.2 Software

ModusToolbox<sup>™</sup> software 3.2 or above.

After installing the software, see the ModusToolbox<sup>™</sup> tools package user guide to get an overview of the software.

### 5.2 Using these instructions

These instructions are grouped into several sections. Each section is dedicated to a phase of the application development workflow. The major sections are:

- **1.** Create a BSP for your board
- **2.** Create a new application
- 3. View and modify the design configuration
- 4. Write firmware
- **5.** Build the application
- 6. Program the device
- 7. Test your design



If you are familiar with developing projects using ModusToolbox<sup>™</sup>, you can use one of the supported starter applications for your kit, such as **Hello World** or **Blinky** directly. This starter application is a complete project, which can run on supported kits without any additional code or configuration. This design is developed for the kits listed in Table 7. You can test this example by selecting the appropriate kit while creating the application. You can go through the instructions in the README.md file and observe how the steps are implemented in the code example.

Even if you are creating a different application from scratch following the instructions in this application note, you can use this code example as a reference.

## 5.3 About the design

This design uses the PSOC<sup>™</sup> 4 MCU to blink an LED. On kits that support UART, the "Hello World" message is printed to the serial port stream.

## 5.4 Create a BSP for your board

All ModusToolbox<sup>™</sup> applications require a target BSP. Infineon provides BSPs for all of our kits (including the kits mentioned in Table 7) and for each chip architecture to use as a starting point. When working with your own hardware, you can modify an Infineon BSP to match the hardware. The BSP Assistant helps to simplify the process. If you are developing for your own hardware, create a custom BSP by following the steps given in ModusToolbox<sup>™</sup> BSP Assistant user guide. Section Opening the Device Configurator describes how the configuration of the custom BSP can be edited.

## 5.5 Create a new application

This section takes you on a step-by-step guided tour of the new application process. It uses the **Empty PSOC4 App** starter application and manually adds the functionality from the **Hello World** starter application. The Eclipse IDE for ModusToolbox<sup>™</sup> is used in the instructions, but you can use any IDE or the command line if you prefer.

If you are familiar with developing projects with ModusToolbox<sup>™</sup> software, you can use the **Hello World** starter application directly. It is a complete design, with all the firmware written for the supported kits. You can walk through the instructions and observe how the steps are implemented in the code example.

If you start from scratch and follow all the instructions in this application note, you can use the **Hello World** code example as a reference while following the instructions.

Launch the Dashboard 3.2 application to get started.

*Note:* Dashboard 3.2 application needs access to the internet to successfully clone the starter application onto your machine.

The Dashboard 3.2 application helps you get started using the various tools with easy access to documentation and training material, a simple path for creating applications and creating and editing BSPs.

**1.** Open the Dashboard 3.2 application.

To open the Dashboard 3.2 application, do one of these:

- Windows: Navigate to [ModusToolbox installation path]/tools\_3.2/dashboard/dashboard.exe Or you can also select the "dashboard" item from the Windows Start menu.
- Linux: [ModusToolbox installation path]/tools\_3.2/dashboard and run the executable
- macOS: Run the "dashboard" app
- 2. On the Dashboard 3.2 window, in the right pane, in the Target IDE drop-down list, select Eclipse IDE for ModusToolbox™, and click Launch Eclipse IDE for ModusToolbox™.



File Help Learn		Franciska (Switch 2049)	Create Create a new amiintion for
() () () () () () () () () ()	ModusToolbox** Documentation	Faing Materia	Target IDE Eclipse IDE for ModusToolbox**   Launch Eclipse IDE for ModusToolbox*  This option opens the Eclipse IDE for ModusToolbox*  This option opens the Eclipse IDE. To create an application, select the "New Application" option in the Eclipse IDE Quick Panel.
Viele Tutorials	Community Support	Sign up for News	Create or edit a Board Support Package (ISP) Create or edit a Board Support Package (ISP) Launch BSP Assistant This option will launch the ModuaToolbox** BSP Assistant tool. ISSP Assistant User Guade
			Install ModusToolbox Setup is not installed. Use the following link to install it:

Figure 11 Dashboard 3.2 application

#### 3. Select a new workspace.

At launch, Eclipse IDE for ModusToolbox<sup>™</sup> displays a dialog to choose a directory for use as the workspace directory. The workspace directory is used to store workspace preferences and development artifacts. You can choose an existing empty directory by clicking the **Browse** button, as shown in the following figure. Alternatively, you can type in a directory name to be used as the workspace directory along with the complete path, and the IDE will create the directory for you.

Eclipse IDE for Modus foolbox	™ 3.2 Launcher			
select a directory as worksp	oace			
Eclipse IDE for ModusToolbox™	3.2 uses the workspace directory to stor	re its preferences and developm	ent artifac	cts.
C:\mtw			~	<u>B</u> rowse
_	not ask again			
Use this as the default and do				
<u>U</u> se this as the default and do <b>Recent Workspaces</b>				
<u>U</u> se this as the default and do <b>Recent Workspaces</b>				

#### Figure 12 Select a directory as the workspace

#### 4. Create a new ModusToolbox<sup>™</sup> application.

- **a.** Click **New Application** in the Start group of the Quick Panel.
- **b.** Alternatively, you can choose **File** > **New** > **ModusToolbox**<sup>™</sup> **Application**, as shown in the following figure.

The Project Creator opens.



mtw - Eclipse IDE for ModusToolt	X00X <sup>™</sup>		-	$\Box$ $\times$	
le Edit Navigate Search Projec	t Run Window Help				
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Figure 13 Create a new ModusToolbox<sup>™</sup> application

#### 5. Select a target PSOC<sup>™</sup> 4 development kit

ModusToolbox<sup>™</sup> speeds up the development process by providing BSPs that set various workspace/ project options for the specified development kit in the new application dialog.

- a. In the **Choose Board Support Package (BSP)** dialog, choose the **Kit Name** that you have. The steps that follow use **CY8CPROTO-040T**. See Figure 14 for help with this step
- b. Click Next



atings Help				
Source Template				
Enter filter text			🛛 Create from MPN Browse for BSP 📄 🕀	CY8CPROTO-040T
Kit Name         AIROC <sup>™</sup> Bluetooth® BSPs           > AIROC <sup>™</sup> Bluetooth® BSPs           > MROC <sup>™</sup> Bluetooth® BSPs           > PMG BSPs           > PSOC <sup>™</sup> 4 BSPs           CY8CKIT-04T           CY8CKIT-04T           CY8CKIT-04T           CY8CKIT-04T           CY8CKIT-04SS           CY8CKIT-04SS           CY8CKIT-04SS           CY8CKROT0-040T           CY8CROT0-040T-MS           CY8CPROT0-040T-MS           CY8CPROT0-040T-MS	MCU/SOC/SIP CY8C4046LQI-T452 CY8C4146AZI-S433 CY8C4149AZI-S433 CY8C4149AZI-S438 CY8C44149AZI-S438 CY8C44147AZI-S435 CY8C44147AZI-S435 CY8C4147AZQ-T495 CY8C4146LWE-HVS155X CY8C4146LWE-HVS155X CY8C4149AZE-S598	Connectivity <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none> <none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none></none>	A	The PSOC <sup>™</sup> 4000T CAPSENSE <sup>™</sup> Prototyping Kit enables you to evaluate and develop with Cypress <sup>2</sup> fifth-generation, low-power CAPSENSE <sup>™</sup> solution using the PSOC <sup>™</sup> 4000T device. Kit Features: • World's Most Reliable, Lowest Power CAPSENSE <sup>™</sup> Solution • On-board Programmer and Debugger Kit Contents: • CY8CPROTO-040T PSOC <sup>™</sup> 4000T CAPSENSE <sup>™</sup> Prototyping Kit • Quick Start Guide
inished loading the manifest data (4	566 ms)			
error(s),				
ummary:				
SP: CY8CPROTO-040T				
ress "Next" to select application				В



- **c.** In the **Select Application** dialog, select **Empty App** starter application, as shown in the following figure.
- **d.** In the **Name** field, type in a name for the application, such as **Hello\_World**. You can choose to leave the default name if you prefer.
- e. Click **Create** to create the application, as shown in the following figure, wait for the Project Creator to automatically close once the project is successfully created.



ettings Help							
Application(s) Root Path:	C:/mtw						Browse
Target IDE:	Eclipse IDE for ModusTo	olbox™					$\sim$
Enter filter text	R	Browse for App	lication	V 🗱 🗄 E	Ē	This empty application provides a template for creating ap	plications using
Template Application	C	New A D	on Name	New BSP Name	1	PSOC™4 devices.	
Empty PSOC4	App	Hello World		APP CY8CPROTO-0	)		
Hello World					-		
Power Modes							
<ul> <li>Peripherals</li> </ul>					- 11		
Emulated EEPR	OM				- 11		
GPIO Interrupt					- 11		
GPIO Pins					- 11		
I2C Master Ezi2	C Slave				- 11		
I2C Slave Using	Callbacks				- 11		
Periodic Interru	upt Using TCPWM				- 11		
PSOC'4 Basic d	evice firmware upgrade				- 11		
SPI Master							
SPI Slave							
TCPWM event	counter						
TCPWM square	wave						
Summary:							
BSP: CY8CPROTO-040T							
Template Application(s): Em	pty PSOC4 App						
Application(s) Root Path: C:	/mtw						
D	- I and a set for the the						
Press Create to create the	selected application(s).						
						F	
						Rack Cross	the Chart

#### Figure 15 Choose starter application

You have successfully created a new ModusToolbox<sup>™</sup> application for a PSOC<sup>™</sup> 4.

The BSP uses CY8C4046LQI-T452 as the default device that is mounted on the PSOC<sup>™</sup> 4 CY8CPROTO-040T Prototyping Kit.

If you are using custom hardware based on PSOC<sup>™</sup> 4, or a different PSOC<sup>™</sup> 4 part number, please refer to the Create a BSP for your board or the BSP Assistant user guide.

## 5.6 View and modify the design configuration

Figure 16 shows the ModusToolbox<sup>™</sup> Project Explorer displaying the structure of the application project.





For understanding the files and folders in detail, see Section 2.4.2 in ModusToolbox™ tools package user guide.



## 5.6.1 Opening the Device Configurator

You can modify the device configurations which is loaded by the selected BSP. For example, default kit BSPs do not have UART enabled. Below steps show how to enable UART peripheral for "Hello World" printing operation and how to enable User LED for PSOC<sup>™</sup> 4 kits.

1. As shown in Figure 17, click **Device configurator** in the **Quick Panel** under the **BSP Configurators** section. This opens the Device Configurator dialog(Figure 18). You can also open the other configurators and configure as required.

☑ Quick Pa (x)= Variables of free Exp	oress 嚕 Breakp 🗖	
• BSP Configurators (APP_CY80	CKIT-041S-MAX)	^
CAPSENSE <sup>™</sup> Configurator CAPSENSE <sup>™</sup> Tuner		i
Smart I/O Configurator	(new configuration)	~



Opening the Device Configurator

Were Configurator		_				- 0	×
File Edit Settings View Help	Resource						
CY8C4046LQI-T452	Catergories Par	e	Serial Communication Block (SCB) 0 (CVI	BSP_UART) - Parameters			đΧ
Peripherals Pins Analog-Routing	System Peripheral-C	locks	Enter filter text			<i>I</i> 5 7	
Enter filter text List of Resources		🖉 y e e 🖌 🗎 🖻	Name	Value	Parameters Pane		
Resource	Name(s)	Personality	✓ Peripheral Documentation		/		- 1
<ul> <li>Communication</li> </ul>		( ciseriality	⑦ Configuration Help	Open UART (SCB) Documentation			
Serial Communication Block (SCE	B) 0 CYBSP UART	UART-1.0 V	✓ General				
Serial Communication Block (SCE	B) 1 scb 1		⑦ Com Mode	Standard			$\sim$
✓ Digital			⑦ Enable LIN Mode				
Timer, Counter, and PWM (TCPWM)	0		⑦ Baud Rate (bps)	115200			
TCPWM 16-bit Counter 0	tcpwm_0_cnt_0		⑦ Oversample	12			~
TCPWM 16-bit Counter 1	tcpwm_0_cnt_1		⑦ Bit Order	LSB First			~
✓ System			⑦ Data Width	8 bits			~
🛩 🛃 CapSense	CYBSP_CAPSENSE	CapSense-1.0 🗸	Parity	None			~
SCLP 0	CYBSP_MSC	MSCLP-3.0 V	(?) Stop Bits	1 bit			~
Watchdog Timer (WDT)	srss_0_wdt_0		(?) Enable Digital Filter				
			✓ Support RS-485				
			⑦ TX-Enable				
			✓ Flow Control				
			⑦ Enable Flow Control				
			✓ Connections	(			_
			2 Clock	d? 🦲 16 bit Divider 0.clk [USED]	Code Preview		
			Code Preview		Pane		đΧ
			Enter search text				0
			<pre>/*  * NOTE: This is a preview only  * cycfg_peripherals.c and cycf  * C:/mtw/Hello_World/bsps/TARG  */</pre>	7. It combines elements of the g_peripherals.h files located in ET_APP_CY8CPROID-040T/config/Gene	the folder: eratedSource		
			<pre>#include "cy_scb_uart.h" #include "cy_scb_uart.h"</pre>				
		Notice List Pane	Vincinde Cy Systix.n				
lotice List							с, ×
😢 0 Errors 🛛 🚹 0 Warnings 🛛 🗐 0 Tasl	ks 🚺 0 Infos						
Fix Description		F	ix Description				Location
Ready							

Figure 18

Overview of design.modus



From the **Resource Categories Pane** of the **Device Configurator** dialog, you can choose different resources to configure, such as peripherals, pins, and clocks.

The **Peripherals** tab shows a list of available peripherals in the device. The configuration in the **Personality** column defines the behavior of the resource. For example, a **Serial Communication Block (SCB)** resource can have **EZI2C, I2C, SPI**, or **UART** as personalities. The **Name(s)** field is the user-defined name of the resource, which is used in firmware development. You can specify one or more names for each pin, as ModusToolbox<sup>™</sup> provides the ability to assign different aliases to the pins, corresponding to different run-time configurations. Note that the listed names must be separated by commas with no space.

In the **Parameters** pane, you can enter the configuration parameters for each enabled resource and the selected personality. The **Code Preview** pane shows the configuration code generated for the selected configuration parameters. This code is populated in the cycfg\_ files in the GeneratedSource folder. Any errors, warnings, and information messages, caused by the configuration, are displayed in the **Notice List** pane.

2. Enable UART peripheral and configure the corresponding clocks as explained in the following steps:

*Note:* For the CY8CKIT-040T kit skip these steps because UART is not supported on this kit.

a. Go to the **Peripherals** tab in **Resources Categories** pane and enable **Serial Communication Block (SCB) 0**, set personality as UART-1.0 and the name as "CYBSP\_UART". In Figure 19, SCB instance 0 is selected based on Rx/Tx pin required for the kit. As shown in Figure 20, the dropdown of Rx and Tx configuration parameters shows pins supported by SCB 0. See the device datasheet for the pins available for each SCB instance.

Res	source	Name(s)	Personality
~	Communication		
	Serial Communication Block (§	SCB) 0 CYBSP_UART	UART-1.0 $\sim$
	Serial Communication Block (Section 2014)	SCB) 1 scb_1	
~	Digital		
	> Timer, Counter, and PWM (TCPW)	v1) 0	
~	System		
	🗸 🔽 CapSense	CYBSP_CAPSENSE	CapSense-1.0 <
	🛃 🗐 MSCLP 0	CYBSP_MSC	MSCLP-3.0 V
	Watchdog Timer (WDT)	srss_0_wdt_0	

#### Figure 19 Enabling SCB as UART

**b.** Set the required configuration parameters such as **Clock**, **Rx**, and **Tx** in the **Parameter** pane. Retain the default values for other parameters.



nter filter text	🖉 😈 🝸 🖻 🛙
lame	Value
Peripheral Documentation	
⑦ Configuration Help	Open UART (SCB) Documentation
General	
⑦ Com Mode	Standard
② Enable LIN Mode	
⑦ Baud Rate (bps)	115200
⑦ Oversample	12
⑦ Bit Order	LSB First
⑦ Data Width	8 bits
Parity	None
⑦ Stop Bits	1 bit
② Enable Digital Filter	0
Support RS-485	
⑦ TX-Enable	
Flow Control	
⑦ Enable Flow Control	
Connections	
⑦ Clock	ළ 16 bit Divider 0 clk [USED]
RX	P2[2] digital_inout (CYBSP_I2C_SCL, CYBSP_DEBUG_UART_RX) [USED]
🕐 тх	🖉 🥚 P2[3] digital_inout (CYBSP_I2C_SDA, CYBSP_DEBUG_UART_TX) [USED]
Actual Baud Rate	
Actual Baud Rate (bps)	114285
⑦ Baud Rate Accuracy (%)	0.794
ode Preview	Ð
nter search text	(
* * NOTE: This is a preview or * cycfg_peripherals.c and cy * C:/mtw/Hello_World/bsps/TA	ly. It combines elements of the cfg_peripherals.h files located in the folder: RGET_APP_CY8CPROTO-040T/config/GeneratedSource

Figure 20

Setting UART configuration parameter

c. Go to the **Peripheral-Clocks** tab in **Resource Categories** pane to configure the clock for UART peripheral.


ile Edit Settings View Help	
CY8C4046LQI-T452	16 bit Divider 0 - Parameters
Peripherals Pins Analog-Routing System Peripheral-Clocks	Enter filter text 2 🗸 🗸 🗸
nter filter text	🖉 🍸 🖻 🖶 🤸 🗎 🖍 Name Value
Resource Name(s) Personality	✓ Peripheral Documentation
16 bit	⑦ Configuration Help Open Peripherals Clock Dividers Documentation
16 bit Divider 0 peri_0_div_16_0 Peripheral Clock-1.0	General
16 bit Divider 1 peri_0_div_16_1	Source Clock     HFCLK (48 MHz ± 2%)
< 16.5 bit	Divider Calculation Manual
16.5 bit Divider 0 peri_0_div_16_5_0	O Divider 35
24.5 bit	② Achieved Frequency 1.371 MHz ± 2%
24.5 bit Divider 0 peri_0_div_24_5_0	(2) Start on Reset
	(2) Peripherals (2) Peripherals (2) Serial Communication Block (SCB) 0 clock (CYBSP_UART) [USED]
	Code Proview
	Code Preview Enter search test
	CodeProview Entersearch tooL. /* DUTE: This is a preview only. It combines elements of the * optig_looks.c and optig_clocks.h files looket in the folder: * optig_looks.c and optig_clocks.h files looket in the folder: * (.rswv/bello.bogs/JAWE/TP_CCFCHOTO-Owthy/enterstedSource * (.rswv/bello.bogs/JAWE/TP_CFCHOTO-Owthy/enterstedSource * (.rswv/bello.bogs/JAWE/TP_CFCHOTO-Owthy/enterstedSource * (.rswv/bello.bogs/JAWE/TP_CFCHOTO-Owthy/enterstedSource * (.rswv/bello.bogs/JAWE/TP_CFCHOTO-Owthy/enterstedSource * (.rswv/bello.bogs/JAWE/TP_CFCHOTO-Owthy/enterstedSource * (.rswv/bello.bogs/JAWE/TP_CFCHOTO-Owthy/enterstedSource * (.rswv/bello.bogs/JAWE/TP_CFCHOTO-Owthy/enterstedSource)* (.rswv/bello.bogs/JAWE/TP_CFCHOTO-Owthy/enterstedSource)* (.rswv/bello.bogs/JAWE/TP_CFCHOTO-Owthy/enterstedSource)* (.rswv/
stre List	Code Proview Enter search torL. /* TOTE: This is a preview only. It combines elements of the * cyctg_clocks.c and cycfg_clocks.h files located in the folder: * cycfg_clocks.c and cycfg_clocks.h
ticeList ● France ▲ O.Warninger.  0.Tacks ▲ D.Infos	Code Preview Enter search tot /* NOTE: This is a preview only. It combines elements of the * cycfg_clocks.c and cycfg_clocks.h files located in the folder: * cycfg_clocks.c and cycfg_Clocks.h files located in the folder: * c/msw/Hello_World/haps/TARGET_APP_CYCCFROTO-040T/config/GeneratedSource */
iotice List	Code Preview Entersearch text. // * NOTE: This is a preview only. It combines elements of the * overfug_clocks.a and cycdg_clocks.h files located in the folder: * C:intw/Bello_Morld/happ/TARGET_APP_CTRCFROTO-0407/config/GeneratedSource *//

#### Figure 21 Configuring clock



Go to the **Code Preview** pane to preview the generated code.

Code Preview	
Enter search text	
/*	
* NOTE: This is a preview only. It combines elements of the	
* cycfg peripherals.c and cycfg peripherals.h files located in the folder:	
* C:/mtw/Hello World/bsps/TARGET APP CY8CPROTO-040T/config/GeneratedSource	
*/	
#include "cv scb uart.h"	
<pre>#include "cv sysclk.h"</pre>	
-1-1	
#if defined (CY USING HAL)	
finclude "cvhal hymgr.h"	
<pre>#endif /* defined (CY USING HAL) */</pre>	
- · · _ · _ · _ · · · · · · · · · · · ·	
#define CYBSP UART HW SCB0	
#define CYBSP UART IRQ scb 0 interrupt IRQn	
const cy_stc_scb_uart_config_t CYBSP_UART_config =	
{	
.uartMode = CY_SCB_UART_STANDARD,	
<pre>.enableMutliProcessorMode = false,</pre>	
.smartCardRetryOnNack = false,	
.irdaInvertRx = false,	
.irdaEnableLowPowerReceiver = false,	
.enableLinMode = false,	
.oversample = 12,	
<pre>.enableMsbFirst = false,</pre>	
.dataWidth = 8UL,	
.parity = CY SCB UART PARITY NONE,	
.stopBits = CY_SCB_UART_STOP_BITS_1,	
.enableInputFilter = false,	
.breakWidth = 11UL,	
.breakLevel = false,	
.dropOnFrameError = false,	
.dropOnParityError = false,	
.receiverAddress = 0x0UL,	
receiverAddressMask = 0x000	

#### Figure 22

#### Code preview pane

**3.** Go to the **Pins** tab in **Resource Categories** pane to configure the GPIO connected to the user LED on the kit. See Table 8 if you are using a different PSOC<sup>™</sup> 4 kit. Configure the GPIO as shown in Figure 23.



le Edit Settings View Help						
Y8C4046LQI-T452				P3[0] (CYBSP_LED2, CYBSP_USE	R_LED2, CYBSP_SW1, CYBSP_USER_BTN)	- Parameters 6
Peripherals Pins Analog-Routing System	Peripheral-Clocks			Enter filter text		🖉 🗗 🍸 🖻
Her filter text           Bource         Name(s)           Port 0         Port 1           Port 2         Port 3           Port 3         Pay 1           Pay 10         PUSP_LED2, CVBSP_USER_LED2, CVBS           Pay 10         CVBSP_SWDCK           Port 4         P4/01 CVBSP_CSD_SEN1           P4/12         CVBSP_CMOD1           P4(3)         CVBSP_CMOD2	1 P2[1] 2 P2[3 3 P2[3] 4 P2[4] 5 P2[5 6 P3[0]	Image: CY8C4046LQI-T452 (24-QFN)	XRES RIGH 17 RIGH 17 RIGH 15 RIGH 13 RIGH 13	Name           > Peripheral Documentation           ⑦ Configuration Help           ③ Indial Drive State           ⑦ Internept Trigger Typ           ○ Output           ⑦ Stew Rate           * Internept Trigger Typ           ○ Output           ⑦ Stew Rate           * Internept Trigger Typ           ○ Output           ⑦ Stew Rate           * Internal Connection           ⑦ Digital Output           ⑦ Digital InOut           ◇ Store Config in Flast	Value Open GPIO Documentation Strong Drive. Input buffer off High (1) CMOS e None Fast <unassigned> <unassign< td=""><td></td></unassign<></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned></unassigned>	
		Et al     B		Code Preview Enter search text /* * opyEq. prins.c. and oper * optimizer. Search text */ */ */ */ */	ev only. It combines elements g pins.h files located in the ps/TARGET_APP_CYSCEROTO-0407/c	of the folder: config/Genera
otice List	os					
Fix Description						Loo

Figure 23 Conf	iguring GPIO
----------------	--------------

Table 8	Pin mapping table across PSOC <sup>™</sup> 4 kits
---------	---

Function	CY8CKIT-14 5 (PSOC™ 4000S)	CY8CKIT-14 9 (PSOC™ 4100S Plus)	CY8CKIT-04 1S-MAX (PSOC™ 4100S Max)	CY8CKIT- 040T PSOC <sup>™</sup> 4000T CAPSENS E <sup>™</sup> Evaluatio n Kit	CY8CPROT O-040T PSOC™ 4000T CAPSENSE™ Prototypin g Kit	CY8CPROT O-040T-MS PSOC <sup>™</sup> 4000T Multi- Sense Prototypin g Kit	CY8CPROT O-041TP CAPSENSE ™ Prototypin g Kit
User LED	P2[5]	P3[4]	P7[3]	P4[0]	1[0], 3[0]	1[0], 3[0]	5[4], 5[5], 6[0], 6[2]

4. Disable (i.e., uncheck) any other peripherals and pins that may have been enabled by default for the kit.

5. Other resources like power, frequency and clock can be configured in the System tab of the Resource Categories Pane. Default Power settings are shown in Figure 24. For this design, no further changes are required.



File Edit Settings	View Help				
CY8C4046LQI-T452			Powe	ver - Parameters	8,
Peripherals Pins	Analog-Routing System	Peripheral-Clocks	Enter	er filter text 🖉 🗸 🗸	80
Enter filter text			🖉 🍸 🖻 🖽 🤸 🖼 🕅 Nam	ne Value	
Resource	Name(s)	Personality	~ D	Documentation	
🗹 Debug	cpuss_0_dap_0	Debug Access-1.0		SysPm API Reference Open SysPm Documentation	
EM_EEPROM	srss_0_eeprom_0		V R	RTOS	
Power	srss_0_power_0	Power Settings-1.0		System idle Power Mode System Deep sleep	
🖌 😰 System Clocks	srss_0_clock_0	SysClocks-2.0		Deep Sleep Latency (ms) 0	-
<ul> <li>High Frequency</li> </ul>				VDDA Voltage (mV) 5000	
HFCLK	srss_0_clock_0_hfclk_0	HFCLK-3.0		VDDD Voltage (mV)     5000	
SYSCLK	srss_0_clock_0_sysclk_0	SYSCLK-1.0		() iebe ienige (iii)	-
✓ Input			OMI		
	srss_0_clock_0_ext_0		8 MH2 + 25		
	srss_U_clock_U_lio_U	ILU-2.0	HICLK SYSLLK 2 48 Mill + 2% 48 Mill + 2%		
Missellaneous	srss_U_clock_U_imo_U	11/10-1.0			
	stres 0, clock 0, lfelk 0	LECLK-10	EXTCLK		
	srss_0_clock_0_itex_tickclk_0				
O STSHER	ana_o_clock_o_anayaticketk_o		0 Hz + 50% 40 Hz + 50% Watchdog Timer (WDT)		
			Code	le Preview	8
			Enter	er search text	
			()		_
			* x	NOTE: This is a preview only. It combines elements of the	
			* *	cycfg_system.c and cycfg_system.h files located in the folder	
			*/	<pre>c./mcw/merio_world/baps/inkdsi_wrr_clocrkoid=0401/conrig/dene.</pre>	aue
				alude Tau augus b"	
					_
Notice List					6
🗙 0 Errors 🔥 0 W	/arnings 🗐 0 Tasks 👔	0 Infos			
Ex Description				1	
Pix Description				L	Catle

#### Figure 24 Configuring System Settings

6. Go to File > Save or press [Ctrl]+[S] to save the configuration and to generate the source code in the GeneratedSource folder.

#### 5.7 Write firmware

This design uses the CM0+ CPU of the PSOC<sup>™</sup> 4 to execute two tasks: UART communication and LED control. The CM0+ CPU uses the UART to print the "Hello World" message to the serial port stream and to make the user LED on the kit blink.

If you are using the **Empty PSOC<sup>™</sup> 4** starter application, you can copy the code snippet provided in this section, to the main.c file of the application project. If you are using the **Hello World** code example, the required files are already in the application.

#### **Firmware flow**

This section explains the code in the main.c file of the application.

In this example, the CM0+ CPU comes out of reset and performs resource initialization. It configures the system clocks, pins, clock to peripheral connections, and other platform resources.

The clocks and system resources are initialized by the BSP initialization function. PDL functions are used to configure and enable the UART peripheral. The UART prints "Hello World" message on the terminal emulator – the onboard KitProg3 acts as the USB-UART bridge to create the virtual COM port. An infinite FOR loop, with a software delay, is used to toggle the user LED periodically.

Note that the application code uses BSP/PDL functions to execute the intended functionality.

- cybsp\_init()- This BSP function initializes the system resources of the device including but not limited to the system clocks and power regulators.
- Cy\_SCB\_UART\_Init() This PDL function initializes the SCB block for UART operation. A configuration structure, CYBSP\_UART\_config, is used as a parameter for this function to configure the UART. This structure is autogenerated by design.modus based on the applied configuration.
- Cy\_SCB\_UART\_Enable() This PDL function enables the SCB block for UART operation.
- Cy\_SCB\_UART\_PutString()- This PDL function places a NULL terminated string in the UART TX FIFO.
- Cy\_GPI0\_Inv()- This PDL function sets a pin output logic state to the inverse of the current output logic state.
- Cy\_SysLib\_Delay()- This PDL function inserts a delay (specified in milliseconds).



Copy Code Listing 1 or Code Listing 2, as applicable, to the main.c of your application project.



#### Code Listing 1 Code snippet with UART communication (main.c) (Use for all kits other than CY8CKIT-040T)

```
* Include header files
#include "cy_pdl.h"
#include "cybsp.h"
* Macros
*****
#define LED_DELAY_MS
                     (500u)
#define CY_ASSERT_FAILED
                     (<mark>0</mark>u)
* Function Name: main
******
* Summary:
* System entrance point. This function performs
* - initial setup of device
* - configure the SCB block as UART interface
 - prints out "Hello World" via UART interface
*
 - Blinks an LED under firmware control at 1 Hz
* Parameters:
* none
* Return:
* int
       ********
int main(void)
{
  cy_rslt_t result;
  cy_stc_scb_uart_context_t CYBSP_UART_context;
  /* Initialize the device and board peripherals */
  result = cybsp_init();
  /* Board init failed. Stop program execution */
  if (result != CY_RSLT_SUCCESS)
  {
     CY_ASSERT(CY_ASSERT_FAILED);
  }
  /* Configure and enable the UART peripheral */
  Cy_SCB_UART_Init(CYBSP_UART_HW, &CYBSP_UART_config, &CYBSP_UART_context);
  Cy_SCB_UART_Enable(CYBSP_UART_HW);
  /* Enable global interrupts */
  __enable_irq();
```



```
/* Send a string over serial terminal */
Cy_SCB_UART_PutString(CYBSP_UART_HW, "Hello world\r\n");
for(;;)
{
    /* Toggle the user LED state */
    Cy_GPI0_Inv(CYBSP_USER_LED1_PORT, CYBSP_USER_LED1_PIN);
    /* Wait for 0.5 seconds */
    Cy_SysLib_Delay(LED_DELAY_MS);
}
```



```
Figure 25
```

**Firmware flowchart** 



Code Listing 2 Code snippet without UART communication (main.c) (Use for any kit including CY8CKIT-040T)

```
* Include header files
#include "cy pdl.h"
#include "cybsp.h"
* Macros
#define LED_DELAY_MS
                   (500u)
#define CY_ASSERT_FAILED
                   (0u)
* Function Name: main
* Summarv:
* System entrance point. This function performs
 - initial setup of device
 - Blinks an LED under firmware control at 1 Hz
*
*
* Parameters:
 none
*
* Return:
 int
*
******
       int main(void)
{
  cy_rslt_t result;
  /* Initialize the device and board peripherals */
  result = cybsp_init();
  /* Board init failed. Stop program execution */
  if (result != CY_RSLT_SUCCESS)
  {
    CY_ASSERT(CY ASSERT FAILED);
  }
  /* Enable global interrupts */
  __enable_irq();
  for(;;)
  {
    /* Toggle the user LED state */
    Cy_GPI0_Inv(CYBSP_USER_LED1_PORT, CYBSP_USER_LED1_PIN);
    /* Wait for 0.5 seconds */
    Cy_SysLib_Delay(LED_DELAY_MS);
```



}

This summarizes how the firmware works in the code example. For details, explore the source files.

# 5.8 Build the application

This section explains how to build the application.

- 1. Select the application project in the Project Explorer window and click the **Build <name> Application** shortcut under the **<name>** group in the Quick Panel. It uses the selected build configuration and compiles/links all projects that constitute the application.
- 2. The **Console** view lists the results of the build operation.



#### Figure 26 Build the application

If there are any errors, check the steps and make sure that you complete all required tasks.

Note: You can also use the CLI to build the application. See the "3.5.3 Use command line" section in the ModusToolbox<sup>™</sup> user guide. This document is located in the /ide\_3.2/docs/ folder in the ModusToolbox<sup>™</sup> installation directory.



# 5.9 Program the device

This section explains how to program the PSOC<sup>™</sup> 4 device.

ModusToolbox<sup>™</sup> uses the SWD protocol to program and debug applications on PSOC<sup>™</sup> 4 devices. For ModusToolbox<sup>™</sup> to identify the device on the kit, the kit must be running KitProg3. Some kits are shipped with KitProg2 firmware instead of KitProg3. ModusToolbox<sup>™</sup> includes the fw-loader command-line tool to switch the KitProg firmware from KitProg2 to KitProg3. See section 5.1.10 KitProg Firmware Loader in the ModusToolbox<sup>™</sup> IDE user guide for more details.

If you are developing hardware on your own, you may need a hardware programmer/debugger; for example, CY8CKIT-005 MiniProg4.

- 1. Connect the kit to the USB port of your computer
- 2. Select the application project and click the **<application name> Program (KitProg3\_MiniProg4)** shortcut under the **Launches** group in the Quick Panel. The IDE will select and run the appropriate run configuration. Note that this step will also perform a build if any files have been modified since the last build.





The Console view lists the results of the programming operation.



🗈 Console X 📳 Problems 🗮 Progress 👖 Memory 🦉 Terminal		*	See.
			0.0
<terminated> Hello_World Program (KitProg3_MiniProg4) [GDB OpenOCD Debugging] openocd.exe (Terminated 12-Aug-2024, 4:20:05 pm)</terminated>			
[ 005] [####################################			
[91%] [####################################			
[94%] [####################################			
[97%] [###################################] [ Programming ]			
[100%] [####################################			
wrote 4480 bytes from file C:/mtw/Hello_World/build/APP_CY8CPROTO-040T/Debug/mtb-example-psoc4-hello-world.hex in 0.742379s (5.893 KiB/s	3)		
** Programming Finished **			
** Program operation completed successfully **			
srst_only separate srst_gates_jtag srst_open_drain connect_deassert_srst			
Info : SWD DPIDR 0x0bcl1477			
shutdown command invoked			
Info : psoc4.dap: powering down debug domain			

Figure 28 Console – programming results

# 5.10 Test your design

This section describes how to test your design.

Once the programming is done, reset the kit and observe the LED blinking.

For kits having UART enabled, follow these steps to observe the "Hello world" being printed. This application note uses Tera Term as the UART terminal emulator to view the results. You can use any terminal to view the output. Skip these steps for CY8CKIT-040T kit as UART is not supported for this kit.

#### 1. Select the serial port

Launch Tera Term and select the USB-UART COM port as shown in Figure 29. Note that your COM port number may be different.

O T CP/ <u>I</u> P	Hos <u>t</u> ; <b>myhost.exa</b>	mple.com	~
	<ul> <li>✓ Hist<u>o</u>ry</li> <li>Service: ○ Telnet</li> <li>● SSH</li> <li>O Other</li> </ul>	TCP <u>p</u> ort#: 22 SSH <u>v</u> ersion: SSH2 IP versio <u>n</u> : AUTO	~
● S <u>e</u> rial	Po <u>r</u> t: COM47: Kit	Prog3 USB-UART (COM47)	· ~

### Figure 29

#### Selecting the KitProg3 COM port in Tera Term

#### 2. Set the baud rate

Go to Setup > Serial port. Set the baud rate to 115200.



Tera Term: Serial port se	etup and connection		×	<					
Port:	COM47	~	<u>N</u> ew setting						
Sp <u>e</u> ed:	115200	~							
<u>D</u> ata:	8 bit	~	Cancel						
P <u>a</u> rity:	none	$\sim$							
<u>S</u> top bits:	1 bit	~	Help						
<u>F</u> low contro	ol: none	~							
Tr	Transmit delay 0 msec/ <u>c</u> har 0 msec/ <u>l</u> ine								
Device Friendly Name: KitProg3 USB-UART (COM47) Device Instance ID: USB\VID_04B4&PID_F155&MI_02\6&1F5FBB6 Device Manufacturer: Cypress Provider Name: Cypress Driver Date: 6-12-2018 Driver Version: 1.9.0.0									

Figure 30

Configuring the baud rate in Tera Term

#### 3. Reset the device

Press the reset switch on the (See Table 9) PSOC<sup>™</sup> 4 kit. A "Hello world" message appears on the terminal. The user LED on the kit will start blinking.

## Table 9 Pin mapping table across PSOC<sup>™</sup> 4 kits for reset switch

Functio n	CY8CKIT-145( PSOC™ 4000S)	CY8CKIT-149( PSOC™ 4100S Plus)	CY8CKIT-041S -MAX(PSOC™ 4100S Max)	CY8CKIT- 040T PSOC™ 4000T CAPSEN SE™ Evaluati on Kit	CY8CPROT O-040T PSOC™ 4000T CAPSENSE ™ Prototypin g Kit	CY8CPR OTO-040 T-MS PSOC <sup>™</sup> 4000T Multi- Sense Prototyp ing Kit	CY8CPR OTO-041 TP CAPSEN SE <sup>™</sup> Prototyp ing Kit
RESET	SW1	SW2	SW1	SW1	SW1	SW1	SW1



M	COM4	7 - Tera	Term VT					_	×
<u>F</u> ile	<u>E</u> dit	<u>S</u> etup	C <u>o</u> ntrol	<u>W</u> indow	<u>H</u> elp				
Hel	lo wo	rld							^
									~

Figure 31





# 6

# My first PSOC<sup>™</sup> 4 design using PSOC<sup>™</sup> Creator

This section:

- Demonstrates how PSOC<sup>™</sup> can be programmed to do more than a traditional MCU
- Shows how to build a simple PSOC<sup>™</sup> design and install it in a development kit.
- Provides detailed steps that make it easy to learn PSOC<sup>™</sup> design techniques and how to use PSOC<sup>™</sup> Creator.

# 6.1 Before you begin

# 6.1.1 Have you installed PSOC<sup>™</sup> Creator?

Download and install PSOC<sup>™</sup> Creator from the PSOC<sup>™</sup> Creator home page. Note that the installation of the toolset may take a long time – see the PSOC<sup>™</sup> Creator Release Notes for more information.

# 6.1.2 Do you have a development kit or prototyping kit?

Testing this design requires one of the kits listed in Table 10, which has an integrated programmer.

		, France, J. Frank, and a sub-based	
Kit name	Kit type	Supported device family	Part number
CY8CKIT-040	Pioneer kit	PSOC <sup>™</sup> 4000	CY8C4014LQI-422
CY8CKIT-042	Pioneer kit	PSOC <sup>™</sup> 4200	CY8C4245AXI-483
CY8CKIT-044	Pioneer kit	PSOC <sup>™</sup> 4200M	CY8C4247AZI-M485
CY8CKIT-046	Pioneer kit	PSOC <sup>™</sup> 4200L	CY8C4248BZI-L489
CY8CKIT-042-BLE	Pioneer kit	PSOC <sup>™</sup> 4200 Bluetooth <sup>®</sup> LE	CY8C4247LQI-BL483
CY8CKIT-045S	Pioneer kit	PSOC <sup>™</sup> 4500S	CY8C4548AZI-S485
CY8CKIT-043	Prototyping kit	PSOC <sup>™</sup> 4200M	CY8C4247AZI-M485
CY8CKIT-145	Prototyping kit	PSOC <sup>™</sup> 4000S	CY8C4045AZI-S413
CY8CKIT-147	Prototyping kit	PSOC <sup>™</sup> 4100PS	CY8C4145LQI-PS433
CY8CKIT-149	Prototyping kit	PSOC <sup>™</sup> 4100S Plus	CY8C4147AZI-S475

Table 10 List of PSOC<sup>™</sup> 4 pioneer kits, prototyping kits, and supported Devices

# 6.1.3 Want to see the project in action?

If you do not want to go through the design process, you can get the completed PSOC<sup>™</sup> Creator project using **Find Code Example** in PSOC<sup>™</sup> Creator (**File > Code Example... > CE230991\_My\_First\_Project**). You can then jump to the Build and Program steps.

# 6.2 About the design

This design simply blinks two LEDs using a TCPWM Component, as shown in Figure 32. The TCPWM is configured in PWM mode. The two complementary outputs of this PWM control the LEDs. The PWM operates at a very low frequency and 50 percent duty cycle so that the toggling of the LEDs is visible. If you use a dual-color LED instead of two separate LEDs, this project can toggle the color of the dual-color LED.





#### Figure 32 My first PSOC<sup>™</sup> 4 design

Γ

# 6.3 Part 1: Create the design

This section takes you on a step-by-step guided tour of the design process. It starts with creating an empty project and guides you through hardware and firmware design entry.

**1.** Start PSOC<sup>™</sup> Creator, and from the **File** menu choose **New** > **Project**, as shown in Figure 33.

	New	•	🔂 E	roject	
	<u>O</u> pen	۲	Ei Ei	le	
	Code Exa <u>m</u> ple				• 4 ×
	A <u>d</u> d	Þ			
	Close Ctrl+F4		pen		
ar'	Close Workspace				





 Select your development kit in the pop-up window. For example, if you have a CY8CKIT-149, select Kit: CY8CKIT-149 (PSOC<sup>™</sup> 4100S Plus) and click Next. If you do not see your PSOC<sup>™</sup> 4 development kit listed in the menu, download and install the kit setup for your kit from the website.

Alternately, you can also select the target device radio button instead of the target hardware and select the appropriate device and click **Next**.

Calact project type		
Choose the type of	project – design, library, or workspace.	
Design project:		
Target kit:	CY8CKIT-149 (PSoC 4100S Plus)	~
<ul> <li>Target module</li> </ul>	e.	
O Target <u>d</u> evice:	:	
Library project		
Workspace		
○ <u>W</u> orkspace		
⊖ <u>W</u> orkspace		

Figure 34

Create a new empty PSOC<sup>™</sup> 4 project

3. Select the option **Empty Schematic** from the next window and click **Next**.



Create Project - CY8CK	T-149 (PSoC 4100S Plus)	? ×
Select project templ Choose a schematic	<b>ate</b> template or start your design with a kit or	example project.
Code example Choose from ou	r library of code examples.	
Pre-populated s	chematic I MCU functions <b>(</b> ike UART, ADC, etc.).	
Empty schemat Create a full cu	iic stom design by adding functionality from	the component catalog.
	< <u>B</u> ack <u>N</u> ex	t > Cancel

**4.** Provide a project name (for example, "My\_First\_Project") and Workspace Name as shown in Figure 36. Choose an appropriate location for your new project, and click **Finish**.



Choose a name a	nd location for your design.					
Workspace:	Create new workspace					
Workspace name:	My_Workspace	1				
Location:	C:\Projects					
Project name:	My_First_Project					

#### Figure 36 Selecting project name and location

5. Creating a new project generates a project folder with a baseline set of files shown in the **Workspace Explorer** (see Figure 37). To open the project schematic file, double-click **TopDesign.cysch**.





#### Figure 37 Opening TopDesign schematic

6. Drag one PWM (TCPWM mode) Component from the Component Catalog onto the schematic, as shown in Figure 38.





#### Figure 38 Location of the PWM Component

7. Double-click the PWM Component on the schematic to configure the Component properties, as shown in Figure 39. Click the PWM tab, and set the Period value to 254 and the Compare value to 127 to generate a PWM signal with a 50 percent duty cycle.

Set the **Prescaler** to 8x, to divide the input clock frequency by 8.



Name: PWM 1							
Configuration	Puiltin						4
Comguration	Duitein						
Prescaler:	8x	$\sim$	Input	Present	Mode		] '
PWM align:	Left align	$\sim$	reload		Rising edge	~	
PWM mode:	PW/M		start		Rising edge	~	
P. J. J.	1 111	-	stop		Rising edge	~	
Dead time cycle:	0	÷	switch		Rising edge	~	
Stop signal event:	Don't stop on kill	$\sim$	count		Level	~	
Kill signal event:	Asynchronous	$\sim$		Regis	ter Swan	RegisterBu	- F
Output line signal:	Direct output	$\sim$	Period	254		65535	
Output line_n signal:	Direct output	$\sim$	Compa	re 127		65535	
Interrupt							_
On terminal count	:						
On compare/capt	ture count						
		DW/M loft al	an e d				
1		PVVIVI, left al	ignea				1

#### Figure 39

#### **Configuring the PWM Component**

8. A PWM Component requires an input clock for its operation. Drag and drop a **Clock** Component onto the schematic, and configure the **Frequency** to 800 Hz by double-clicking on the Component, as shown in Figure 40 and Figure 41. Because the Prescaler value set in PWM Component is 8, the effective input clock of the PWM is only 100 Hz. Therefore, the PWM period of 254 results in a PWM output time period of 2.54 seconds.



A Search for	
Cypress Off-Chip	4 ۵
Cypress Component Catalog	
🗄 🐼 Analog	
🕀 🐼 CapSense	
🕀 🔯 Communications	
🔁 🔯 Digital	
🗈 🐼 Display	
🕀 🐼 Ports and Pins	
🕀 🔯 Power Supervision	
🖨 🐼 System	
Bootloadable [v1.60]	
Bootloader [v1.60]	
Clock [v2.20]	
Die Temperature [v1.0]	
DMA Channel [v1.0]	
Emulated EEPROM [v2.20	]
🗄 🔯 External Memory Interface	e
	/2.10]
Interrupt [v1.70]	
Real-time clock (RTC) [v1.	.30]



Location of the clock Component

Γ	Configure 'Clock_1'
	Name: Clock_1
	Basic Built-in
	Clock type:      New      Existing
	Source: <auto></auto>
	Specify:         Frequency:         800         Hz         ✓           ✓         Tolerance:         5%         +         5%
	Use fractional divider
	Summary API Generated: Yes Uses Clock Tree Resource: Yes
	By default, all clocks are marked as 'start on reset'. The setting can be changed in the Design Wide Resource

Figure 41

**Configuring the clock Component** 

Г



#### 6 My first PSOC<sup>™</sup> 4 design using PSOC<sup>™</sup> Creator

**9.** Drag and drop a **Digital Output Pin** Component. Change the name to LED\_1 as shown in Figure 42 and Figure 43. Add another Digital Output Pin Component and change its name to LED\_2.

	_	
🗎 Search for		
Cypress Off-Chip	٥	₽
Cypress Component Catalog		
🕂 🐼 Analog		
🖶 📷 CapSense		
🖶 🔯 Communications		
🕀 🔯 Digital		
🖻 📷 Display		
🖻 🔯 Ports and Pins		
Analog Pin [v2.20]		
- 🛃 Digital Bidirectional Pi	in [v2.20]	
- B Digital Input Pin [v2.2	0]	
Digital Output Pin [v2	.20]	
🖶 🔯 Power Supervision		
🕂 🐼 System		
🗄 🐼 Thermal Management		

Figure 42

Location of the digital output pin Component



Configure 'LED_1' Name: LED_1 Pins Mapping Clocking	Built-in		? ×
Number of pins: 1 X		Output	
	<ul> <li>Type</li> <li>Analog</li> <li>Digital input</li> <li>HW connection</li> <li>Digital output</li> <li>HW connection</li> <li>Output enable</li> <li>Bidirectional</li> <li>External terminal</li> </ul>	Drive mode Strong drive	Initial drive state: High (1) Min. supply voltage:
·			,
Datasheet	С	OK Apply	Cancel

#### Figure 43 Renaming a pin Component

**10.** In the schematic window, select the wire tool as shown in Figure 44, or press **W**.



Figure 44 Selecting the wire tool

**11.** Wire the Components together, as shown in Figure 45.





Figure 45 Wiring the schematic

12. Most Components are disabled at device reset (the major exception being the Clock Component, which is automatically started as a default), and you must add code to the project to enable them. Open main.c from **Workspace Explorer** and add code to the main() function, as provided in Code Listing 3.

**Code Listing 3 Enabling the PWM Component** 

```
int main(void)
{
   /* Enable and start the PWM */
   PWM_1_Start();
   for(;;)
   {
   }
}
```

**13.** Select **Build My\_First\_Project** from the Build menu. Note that PSOC<sup>™</sup> Creator automatically generates source code files in the Workspace Explorer window for the PWM, Clock, and Digital Output Pin Components, as shown in Figure 46.





**14.** Open the file My\_First\_Project.cydwr (Design-Wide Resource file) from **Workspace Explorer** and click the **Pins** tab. You can use this tab to select the device pins for the outputs LED\_1 and LED\_2.



Figure 47 shows the pin configuration to connect the LED\_1 and LED\_2 pins to the LEDs in the CY8CKIT-149 PSOC<sup>™</sup> 4 prototyping kit. See Table 11 if you are using a different PSOC<sup>™</sup> 4 pioneer kit, or Table 12 if you are using a PSOC<sup>™</sup> 4 prototyping kit.



Figure 47 Pin selection

#### Table 11Pin mapping table across pioneer kits

Funct ion	CY8CKIT-04 0 (PSOC™ 4000)	CY8CKIT-04 1(PSOC™ 4100S)	CY8CKIT-04 2(PSOC™ 4200)	CY8CKIT-04 2- BLE(PSOC <sup>™</sup> 4200 BLE)	CY8CKIT-04 4(PSOC™ 4200M)	CY8CKIT-04 6(PSOC™ 4200L)	CY8CKIT-04 5S(PSOC™ 4500S)
Green LED (Activ e LOW)	P1[1]	P2[6]	P0[2]	P3[6]	P2[6]	P5[3]	P0[0]
Red LED (Activ e LOW)	P3[2] <sup>1)</sup>	P3[4] <sup>2)</sup>	P1[6]	P2[6]	P0[6]	P5[2]	P1[6]

 PSOC<sup>™</sup> 4000 parts have fixed pins for complementary PWM outputs - P1[1] and P1[6]. You cannot use any other pins for PWM outputs. See the device datasheet for more details. If you are using the CY8CKIT-040, you can use the green LED connected to P1[1], as LED1. To use the red LED as LED2, connect P3[2] from header J4 to P1[6] from header J3, using a wire. Alternately, you can connect an external LED to P1[6] as LED2.

Similar to the note above, if you are using the CY8CKIT-041, you can use the green LED connected to P2[6], as LED1 and the complementary PWM output P2[7] for LED2. To use the red LED as LED2, connect P3[4] from header J2 to P2[7] from header J3, using a wire. Alternately, you can connect an external LED to P2[7] as LED2.

Table 12	Pin mapping table across prototyping ki	ts
----------	---	----

Function	CY8CKIT-145 (PSOC™ 4000S)	CY8CKIT-149 (PSOC™ 4100S Plus)
Green LED - LED 1 (Active LOW)	P3[4]	P1[6]



Table 12 (cont	(continued) Pin mapping table across prototyping kits		
Function		CY8CKIT-145 (PSOC™ 4000S)	CY8CKIT-149 (PSOC™ 4100S Plus)
Green LED - LED 2 (Active	LOW)	P3[5]	P5[7]

15. Finally, rebuild the project as explained in Step 13.

#### Part 2: Program the device 6.4

This section explains how to program the device. Connect the kit board to your computer using the USB cable.

Select the PSOC<sup>™</sup> Creator menu item **Debug** > **Select Debug Target**, as shown in Figure 48. 1.

	Windows		•
9934 9934	<u>P</u> rogram Select target and program	Ctrl+F5	
裓	Select Debug <u>T</u> arget		
惫	<u>D</u> ebug	F5	
羝	Debug without Programming	Alt+F5	
燕	Select target and debug		

#### Figure 48

Γ

#### Selecting debug target

2. In the Select Debug Target dialog box, click Port Acquire, and then click Connect, as shown in Figure 49. Click **OK** to close the dialog box.



PSoC 4100S Plus CY8C4147AZI-S475 PSoC 4100S Plus (CortexM0p) Silicon ID: 0x0BC11477 Cypress ID: 0x257C12B5
PSoC 4100S Plus (CortexM0p) Silicon ID: 0x0BC11477 Cypress ID: 0x257C12B5
Revision: PRODUCTION
Target unacquired

#### Figure 49 Connecting to a device

3. Choose the menu item **Debug** > **Program** to program the device with the project, as shown in Figure 50.



#### Figure 50 Programming the device

**4.** You can view the programming status on the status bar (lower-left corner of the window), as shown in Figure 51.



Page 1 Programming - Erasing

## Figure 51 Programming status

**5.** After the device is programmed, ensure that the LEDs toggle, and confirm the working operation of the project.



#### 7 Summary

# 7 Summary

This application note explored the PSOC<sup>™</sup> 4 architecture and development tools. PSOC<sup>™</sup> 4 is a truly programmable embedded system-on-chip, integrating configurable analog and digital peripheral functions, memory, and an Arm<sup>®</sup> Cortex<sup>®</sup>-M0/M0+ microcontroller on a single chip. Because of the integrated features and low-leakage power modes, PSOC<sup>™</sup> 4 is an ideal choice for low-power and cost-effective embedded systems.

This application note also guided you to a comprehensive collection of resources to accelerate in-depth learning about PSOC<sup>™</sup> 4.



#### References

# References

- [1] Infineon Technologies AG: 001-54181: Getting started with PSOC<sup>™</sup> 3; Available online
- [2] Infineon Technologies AG: 001-77759: Getting started with PSOC<sup>™</sup> 5LP; Available online

# **Revision history**



Document revision	Date	Description of changes
**	2013-01-24	New Application Note
*A	2013-04-11	Demo project changed to leverage Pioneer kit. Added architecture introduction.
*В	2013-05-09	Reformatted graphics. Updated links.
*C	2013-12-19	Updated attached Associated Project files. Updated content across the entire document. Updated in new template.
*G	2014-04-10	Updated the projects and the respective section in the AN to support PSOC <sup>™</sup> Creator 3.0 SP1 and PSOC <sup>™</sup> 4000 device.
*H	2014-09-25	Added Code Examples section. Minor edits and format changes throughout the document.
*	2015-03-17	Added More Information section. Removed detailed feature descriptions. Updated for PSOC <sup>™</sup> 4200M family of devices.
*J	2015-09-10	Updated PSOC <sup>™</sup> resources and PSOC <sup>™</sup> is more than an MCU. Added the following sections: Convert Project to Bootloadable for CY8CKIT-049, Bootload Your CY8CKIT-049, and More PSOC <sup>™</sup> 4 Code Examples. Updated Figure 8.
*K	2015-09-16	Updated for PSOC <sup>™</sup> 4200L. Updated the example projects to PSOC <sup>™</sup> Creator 3.3.
*L	2015-12-30	Updated the example projects to PSOC <sup>™</sup> Creator 3.3 SP1.
*M	2016-02-05	Updated for PSOC <sup>™</sup> 4000S and PSOC <sup>™</sup> 4100S. Updated the example projects to PSOC <sup>™</sup> Creator 3.3 SP2. Updated Table 10, Table 11 to add PSOC <sup>™</sup> 4200 BLE.
*N	2017-04-19	Updated logo and copyright
*0	2017-10-06	Added references to PSOC <sup>™</sup> 4100S Plus throughout the document. Updated Table 1 to add PSOC <sup>™</sup> 4100S Plus. Updated PSOC <sup>™</sup> resources with the reference of AN64846 - Getting Started with CAPSENSE <sup>™</sup> .
*P	2017-11-03	Updated the example projects to PSOC <sup>™</sup> Creator 4.2 Updated Table 1 to add supported kit Updated Table 10 to add CY8CKIT-49, CY8CKIT-145 and CY8CKIT-149 Added Table 11 to include CY8CKIT-145 and CY8CKIT-149 pin mapping Updated Figure 7. Added example project of CY8CKIT-145 and CY8CKIT-149 as a part of the AN79953.zip file in this application note landing page.
*Q	2018-03-06	Updated template Updated for PSOC <sup>™</sup> 4100PS Minor edits and format changes throughout the document Added example project of CY8CKIT-147 as a part of the AN79953.zip file

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# **Revision history**

Document revision	Date	Description of changes
*R	2018-05-04	Updated template
		Corrected the link to PSOC <sup>™</sup> 4100S Plus in PSOC <sup>™</sup> resources
*S	2019-09-06	Updated Table 1 to add PSOC <sup>™</sup> 4500 and update the specifications of PSOC <sup>™</sup> 4100S Plus device family.
		Added Motor Control Accelerator feature.
*T	2020-11-09	Updated for ModusToolbox <sup>™</sup> support for some of the PSOC <sup>™</sup> 4 devices.
		Corrected the links in PSOC <sup>™</sup> resources.
		PSOC <sup>™</sup> 4 families are recategorized in Local sales office locations PSOC <sup>™</sup> 4 feature set
		Added new section My first PSOC <sup>™</sup> 4 design using ModusToolbox <sup>™</sup>
		Removed sections : Convert Project to Bootloadable for CY8CKIT-049, Bootload Your CY8CKIT-049, and More PSOC <sup>™</sup> 4 Code Examples
*U	2021-07-08	Updated to Infineon template
		Updated Figure 2, Figure 3, Figure 4, and Figure 5 to the latest MTB 2.3 version
		Updated document with PSOC <sup>™</sup> 4100S Max device
		Changed the default device to PSOC <sup>™</sup> 4100S Max and updated Figure 8
		Updated Modify the design section
*V	2022-06-15	Updated document with PSOC <sup>™</sup> 4000T device
		Updated with the latest release version of ModusToolbox™ (version-3.0)
*W	2023-02-13	Updated Folder structure with the latest release version of ModusToolbox™(VERSION-3.0)
*Х	2023-07-21	Updated the pin changes for PSOC <sup>™</sup> 4000T device
		Updated content with the latest release of ModusToolbox <sup>™</sup> 3.1
*ү	2024-02-05	Fixed broken links
*Z	2024-02-26	Updated content with the latest release of ModusToolbox <sup>™</sup> 3.2
AA	2024-09-18	Changed the default device to CY8CPROTO-040T kit
AB	2025-01-13	Updated the document with CY8CPROTO-040T-MS PSOC <sup>™</sup> 4000T Multi- Sense Prototyping Kit
AC	2025-03-27	Updated document with PSOC <sup>™</sup> 4100T Plus device

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